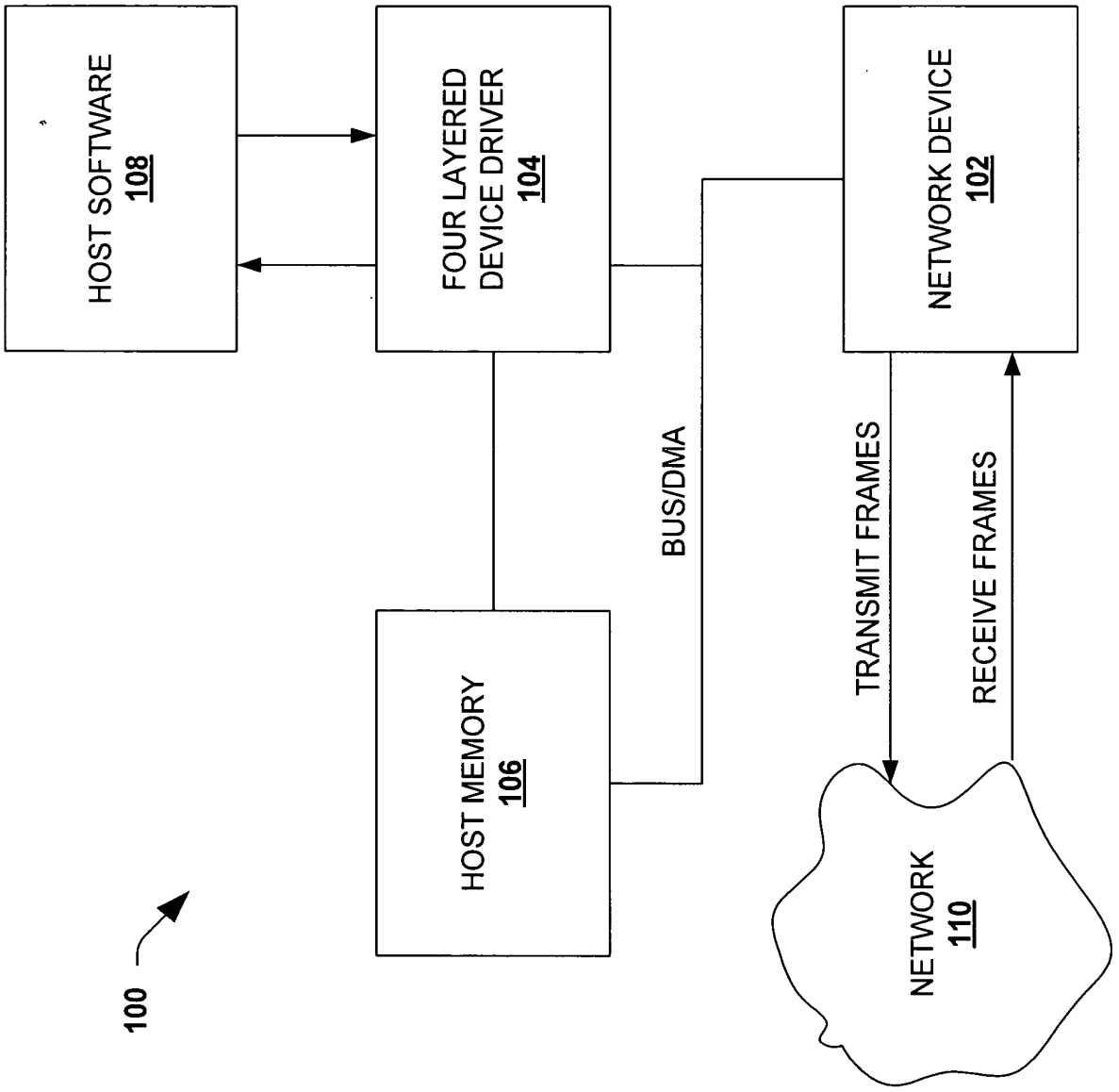
HOST SOFTWARE
108
FOUR LAYERED
DEVICE DRIVER
104
NETWORK DEVICE
102
HOST MEMORY
106
BUS/DMA
TRANSMIT FRAMES
RECEIVE FRAMES
NETWORK
110
100

FIG. 1

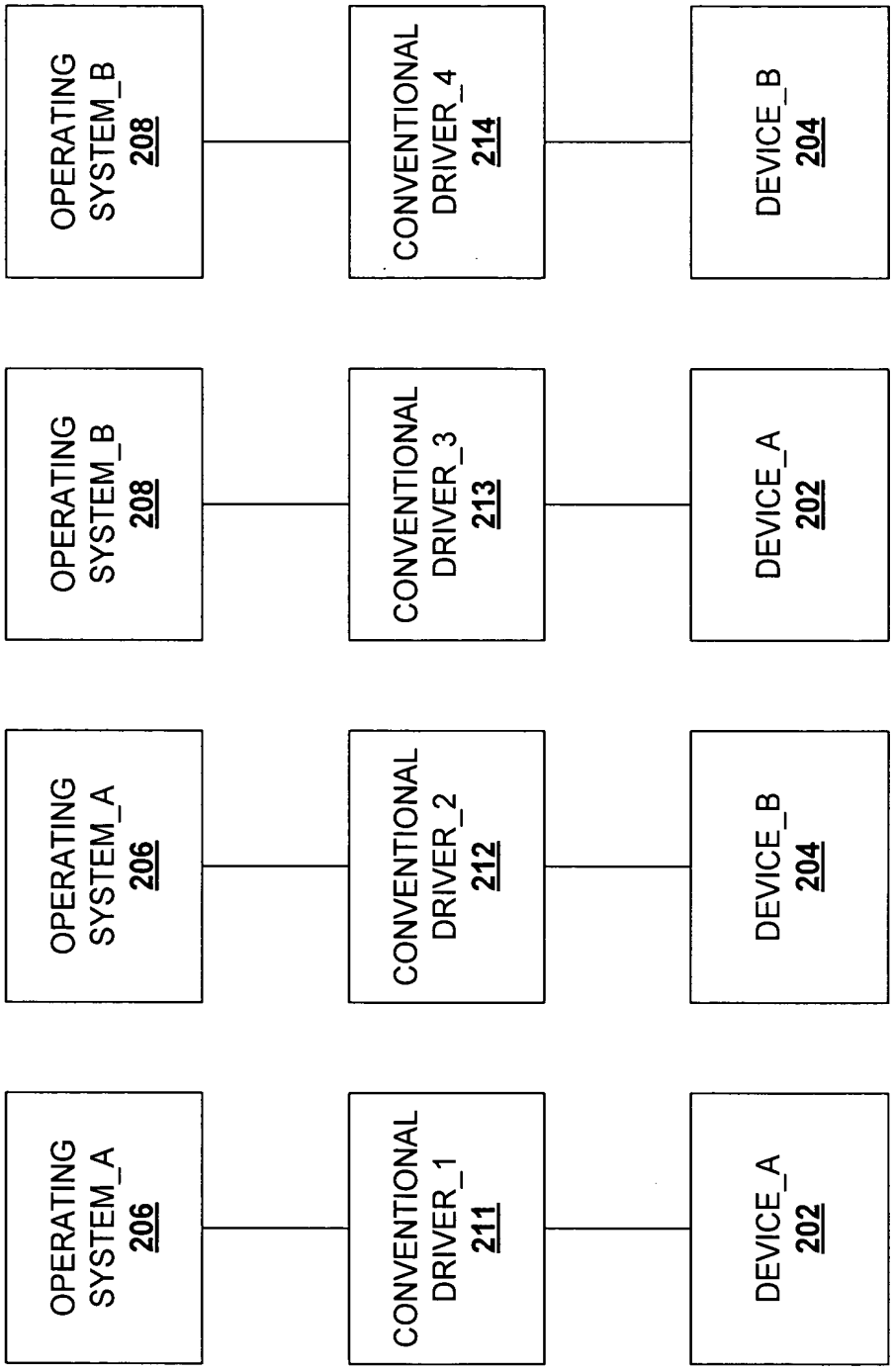
OPERATING SYSTEM_A 206
CONVENTIONAL DRIVER_1 211
DEVICE_A 202
OPERATING SYSTEM_A 206
CONVENTIONAL DRIVER_2 212
DEVICE_B 204
OPERATING SYSTEM_B 208
CONVENTIONAL DRIVER_3 213
DEVICE_A 202
OPERATING SYSTEM_B 208
CONVENTIONAL DRIVER_4 214
DEVICE_B 204

FIG. 2

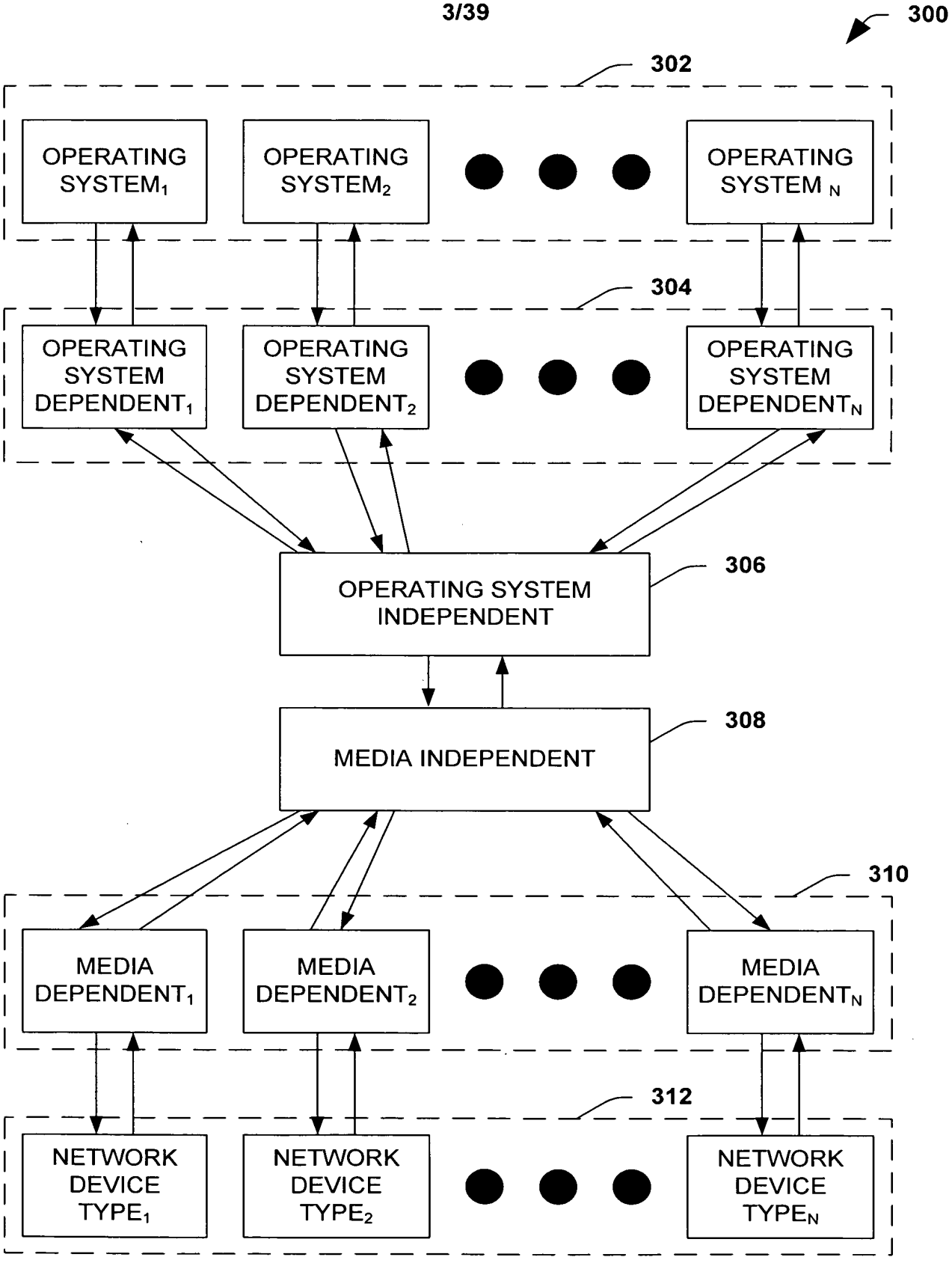
300
302
OPERATING SYSTEM$_1$
OPERATING SYSTEM$_2$
OPERATING SYSTEM $_N$
304
OPERATING SYSTEM DEPENDENT$_1$
OPERATING SYSTEM DEPENDENT$_2$
OPERATING SYSTEM DEPENDENT$_N$
306
OPERATING SYSTEM INDEPENDENT
308
MEDIA INDEPENDENT
310
MEDIA DEPENDENT$_1$
MEDIA DEPENDENT$_2$
MEDIA DEPENDENT$_N$
312
NETWORK DEVICE TYPE$_1$
NETWORK DEVICE TYPE$_2$
NETWORK DEVICE TYPE$_N$

FIG. 3

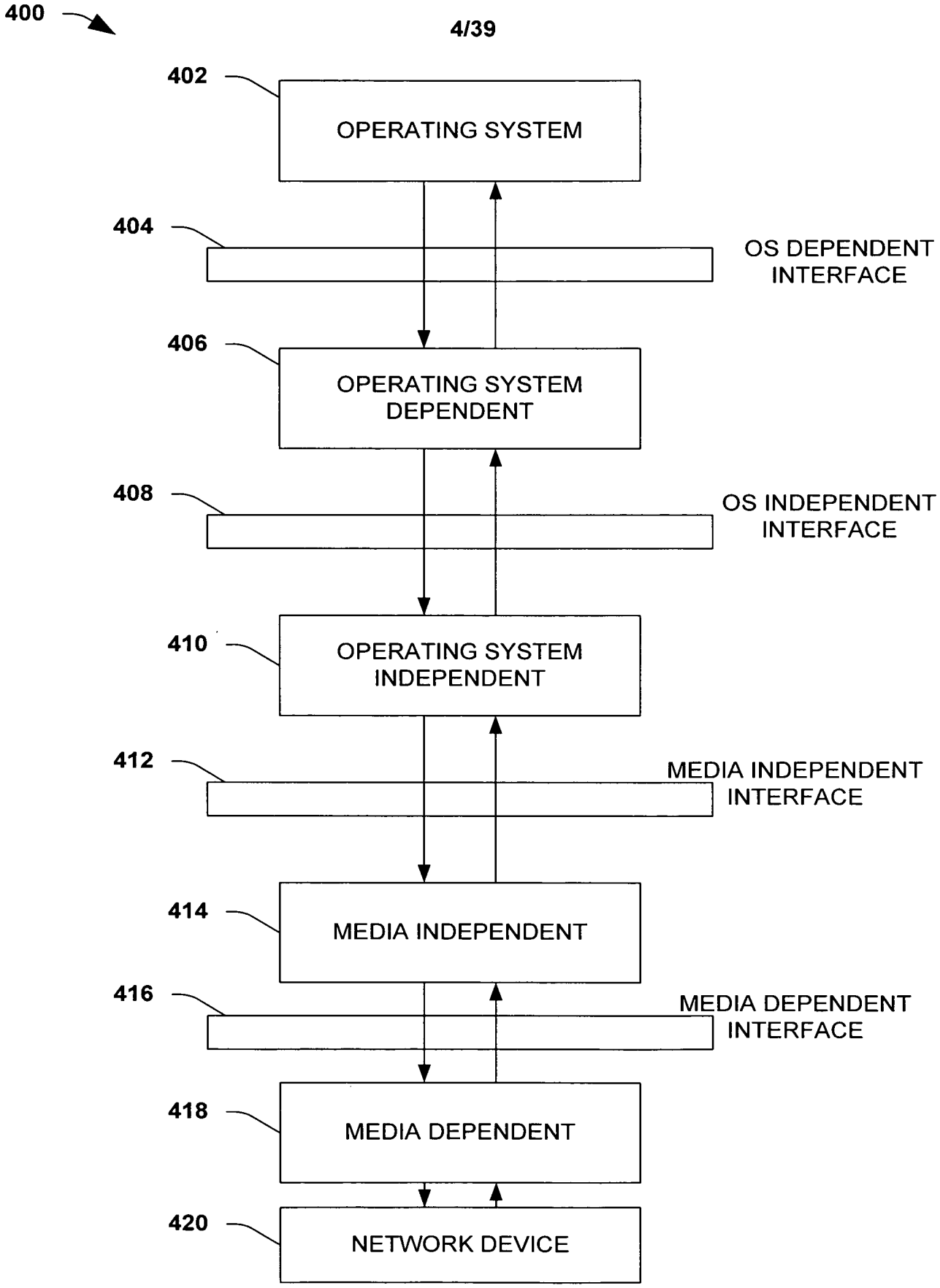
400
402
OPERATING SYSTEM
404
OS DEPENDENT INTERFACE
406
OPERATING SYSTEM DEPENDENT
408
OS INDEPENDENT INTERFACE
410
OPERATING SYSTEM INDEPENDENT
412
MEDIA INDEPENDENT INTERFACE
414
MEDIA INDEPENDENT
416
MEDIA DEPENDENT INTERFACE
418
MEDIA DEPENDENT
420
NETWORK DEVICE

FIG. 4

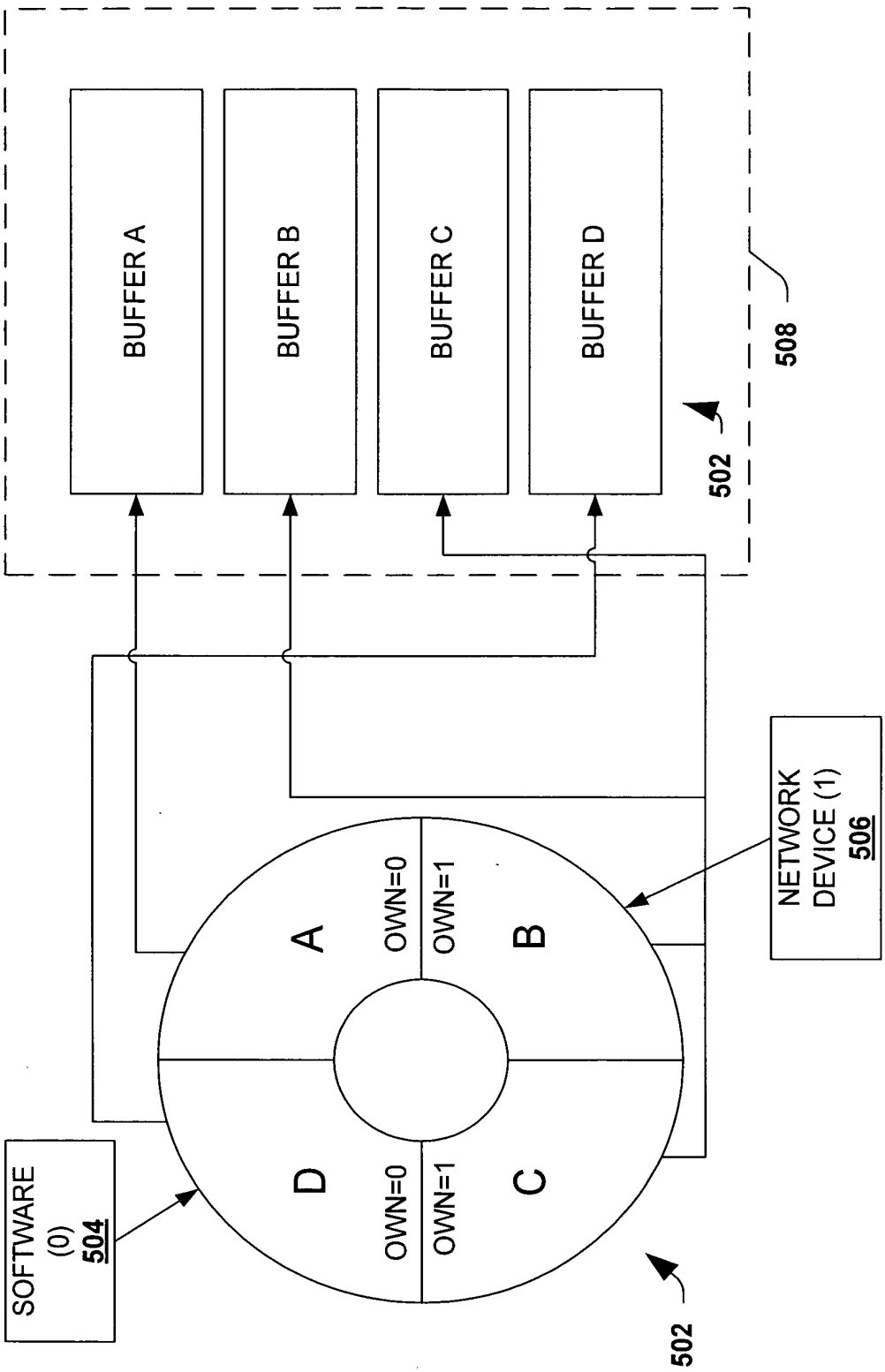
BUFFER A
BUFFER B
BUFFER C
BUFFER D
508
502
A
B
C
D
OWN=0
OWN=1
OWN=0
OWN=1
SOFTWARE
(0)
504
NETWORK
DEVICE (1)
506
502
500

FIG. 5

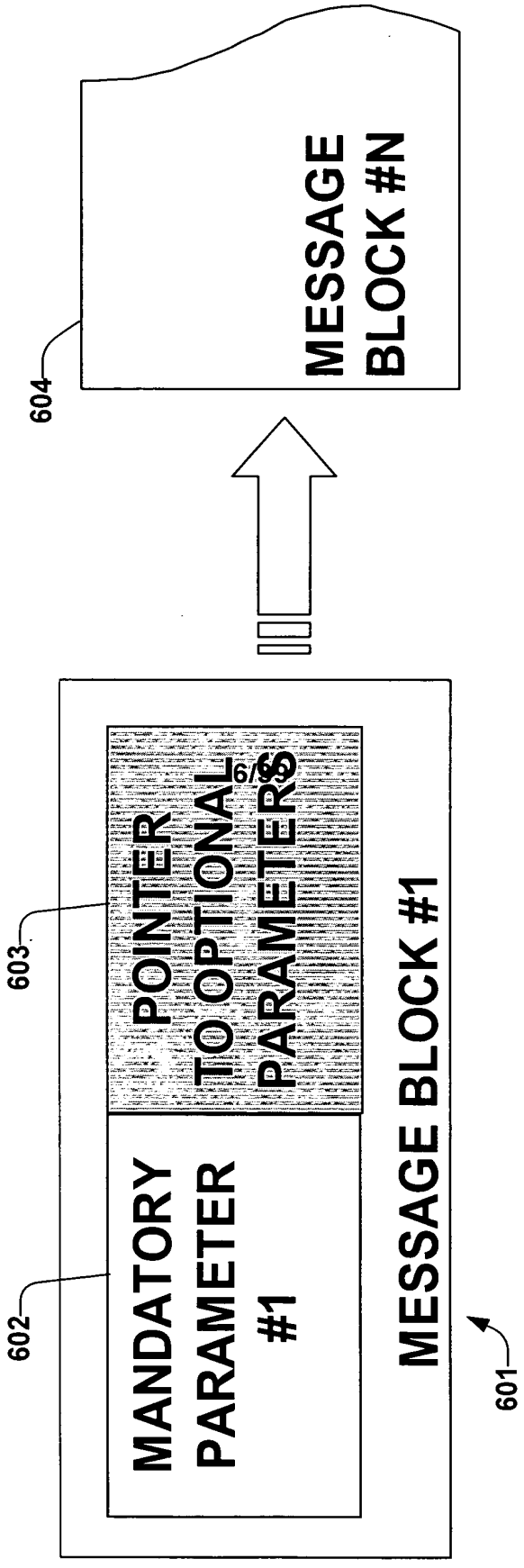
MESSAGE BLOCK #N
604
MESSAGE BLOCK #1
601
MANDATORY PARAMETER #1
602
POINTER TO OPTIONAL PARAMETERS
603

FIG. 6

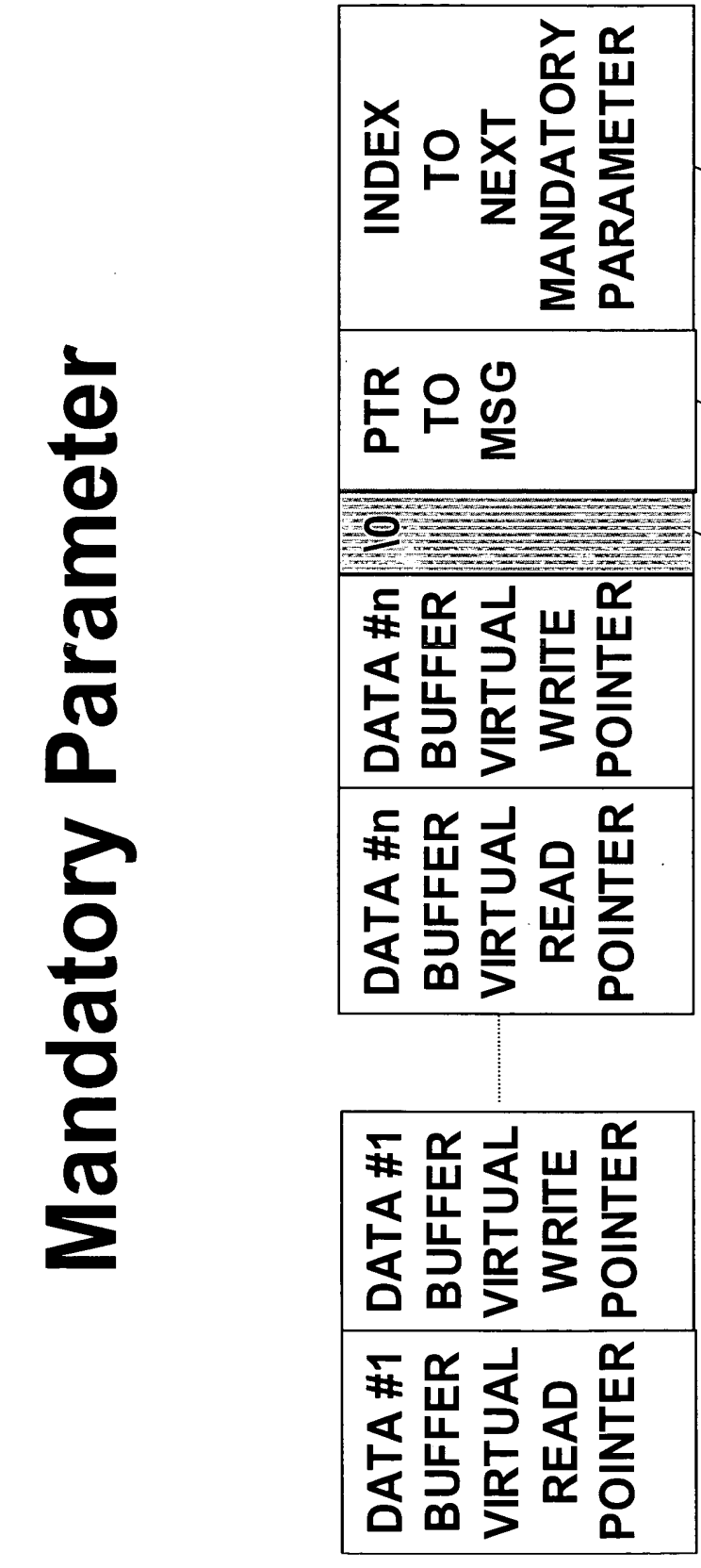
Mandatory Parameter
DATA #1 BUFFER VIRTUAL READ POINTER
DATA #1 BUFFER VIRTUAL WRITE POINTER
DATA #n BUFFER VIRTUAL READ POINTER
DATA #n BUFFER VIRTUAL WRITE POINTER
\0
PTR TO MSG
INDEX TO NEXT MANDATORY PARAMETER
702
704
706
708
700

FIG. 7

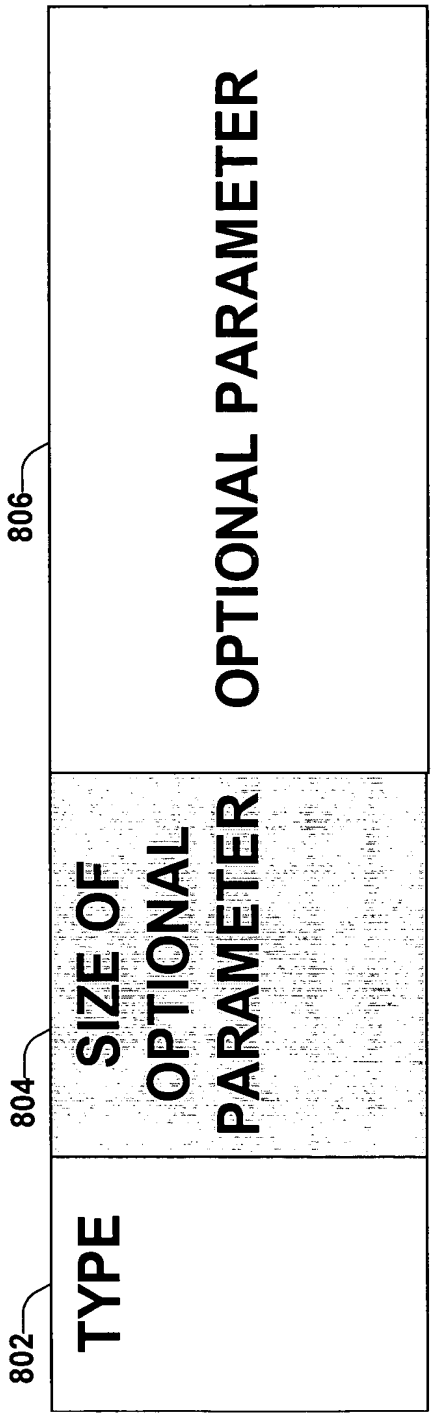
TYPE
SIZE OF OPTIONAL PARAMETER
OPTIONAL PARAMETER
802
804
806
800

FIG. 8

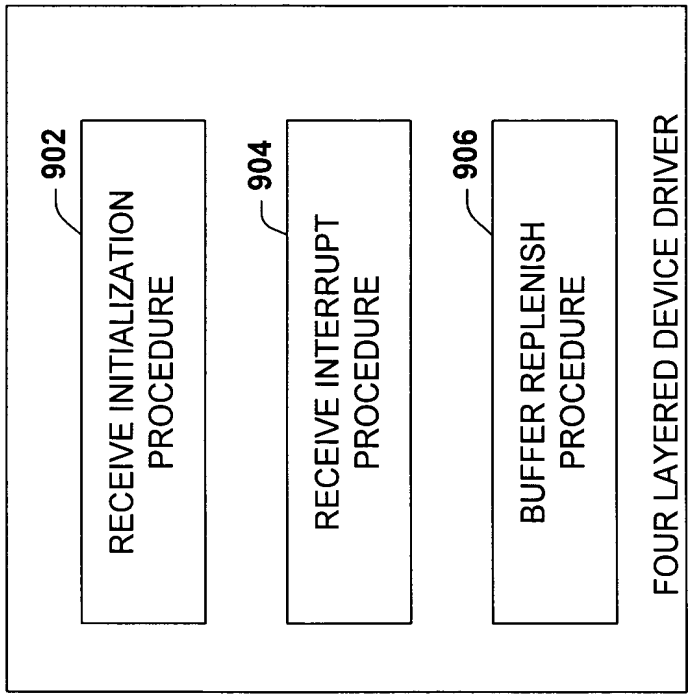
902
RECEIVE INITIALIZATION PROCEDURE
904
RECEIVE INTERRUPT PROCEDURE
906
BUFFER REPLENISH PROCEDURE
FOUR LAYERED DEVICE DRIVER
900

FIG. 9

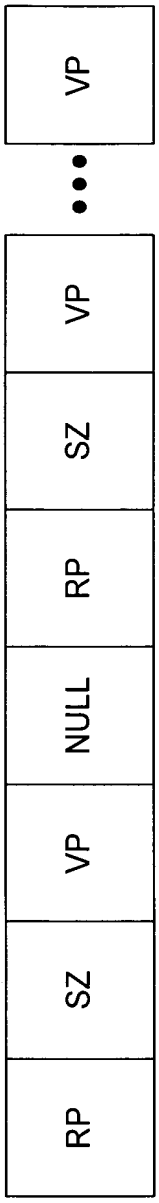
RP
SZ
VP
NULL
RP
SZ
VP
VP

FIG. 10

FIG. 11

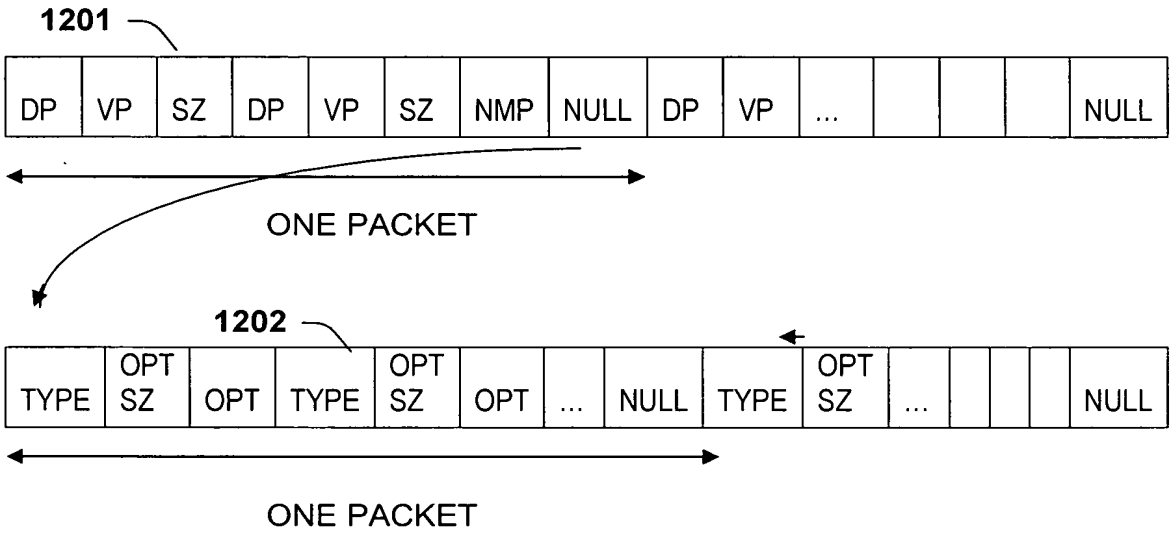

FIG. 12

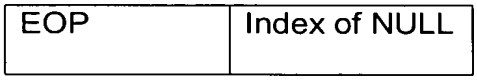

FIG. 13

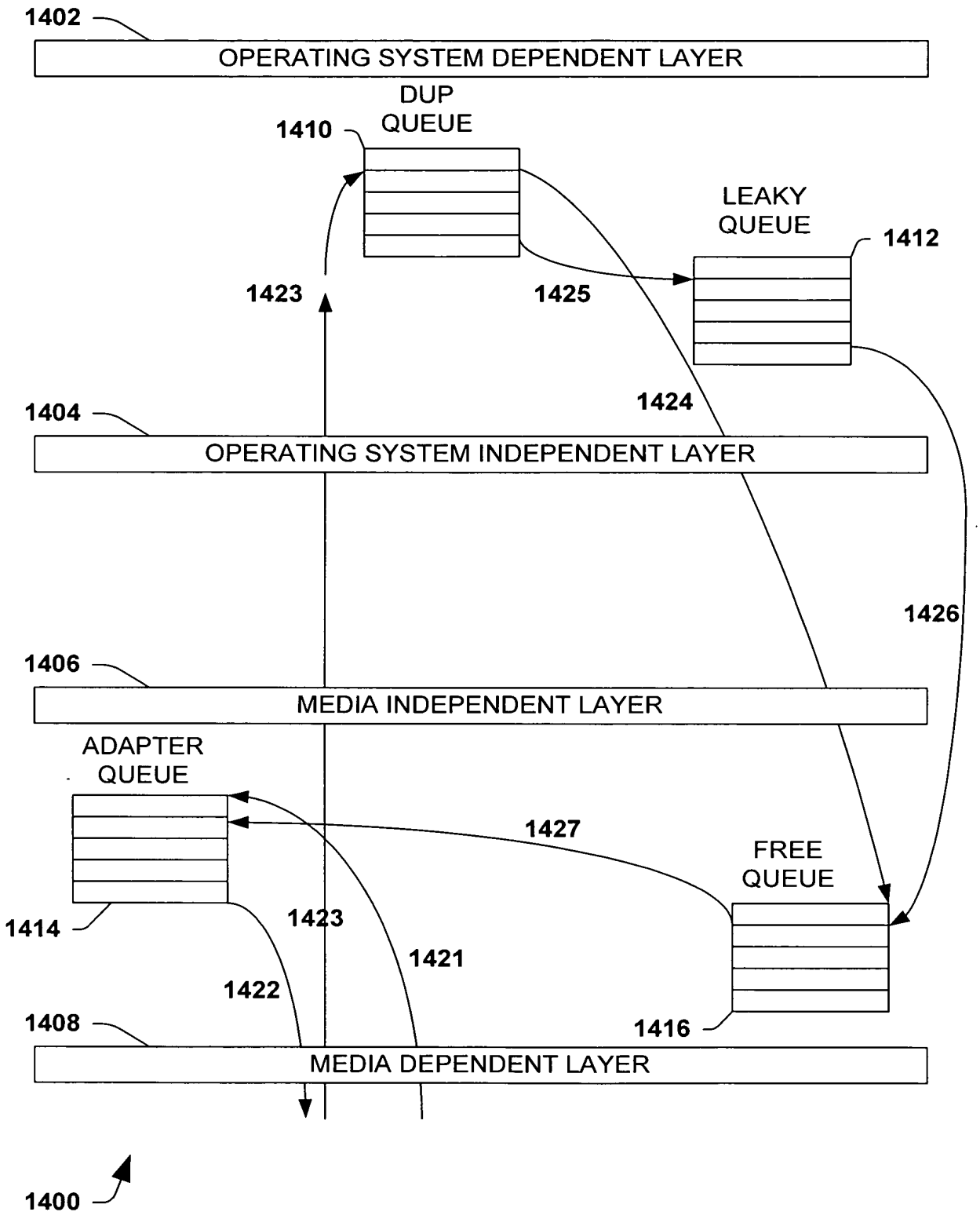
1402
OPERATING SYSTEM DEPENDENT LAYER
DUP
QUEUE
1410
LEAKY
QUEUE
1412
1423
1425
1424
1404
OPERATING SYSTEM INDEPENDENT LAYER
1426
1406
MEDIA INDEPENDENT LAYER
ADAPTER
QUEUE
1427
FREE
QUEUE
1414
1423
1421
1422
1408
1416
MEDIA DEPENDENT LAYER
1400

FIG. 14

ADAPTER QUEUE DATA STRUCTURE 902

BASE ADDRESS POINTERS	SIZE
MANDATORY AND OPTIONAL PARAMETERS	USER SPACE (POINTER TO VOID)

DUPLICATE QUEUE DATA STRUCTURE 904

POINTER TO VA	SIZE
VOID POINTER	

FREE QUEUE DATA STRUCUTRE 906

POINTER TO VA	SIZE

LEAKY QUEUE DATA STRUCTURE 908

POINTER TO VA	SIZE
VOID POINTER	

FIG. 15

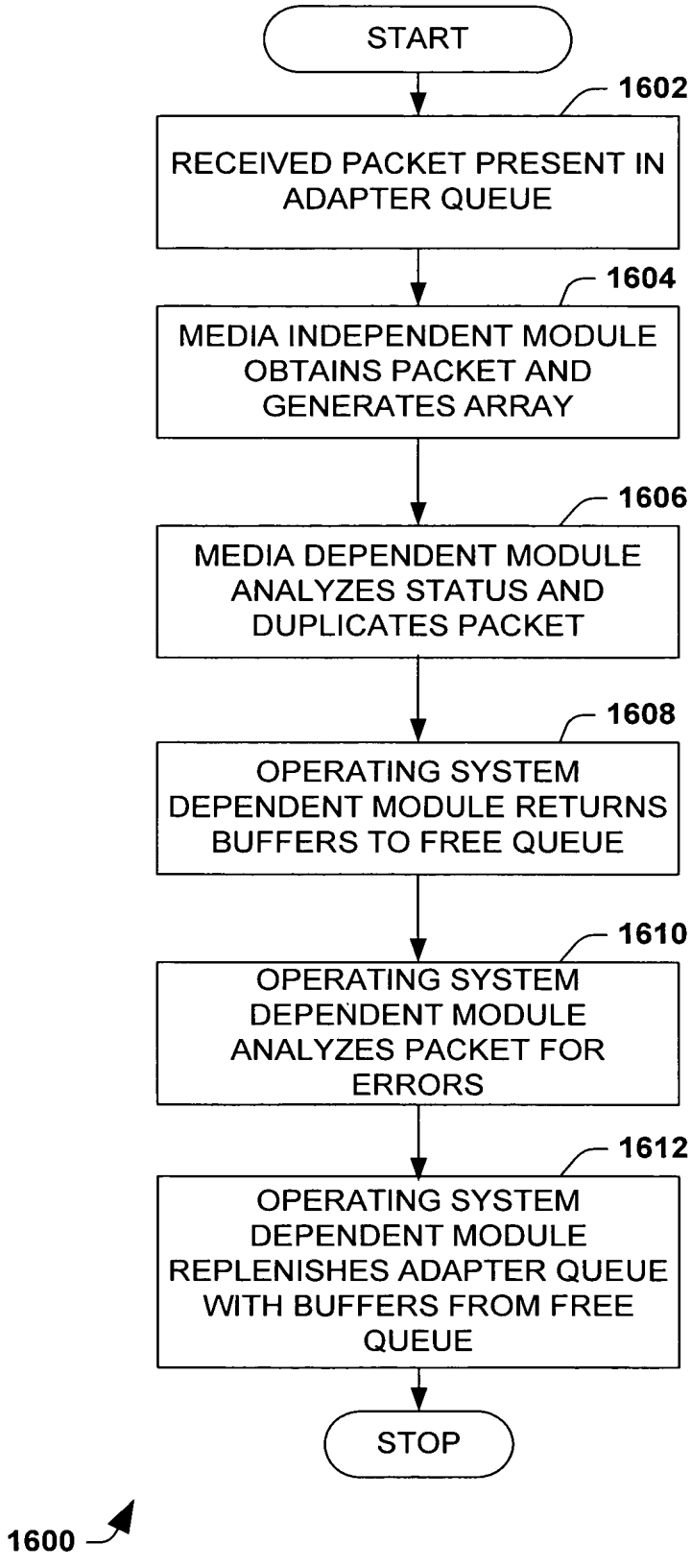
START
1602
RECEIVED PACKET PRESENT IN ADAPTER QUEUE
1604
MEDIA INDEPENDENT MODULE OBTAINS PACKET AND GENERATES ARRAY
1606
MEDIA DEPENDENT MODULE ANALYZES STATUS AND DUPLICATES PACKET
1608
OPERATING SYSTEM DEPENDENT MODULE RETURNS BUFFERS TO FREE QUEUE
1610
OPERATING SYSTEM DEPENDENT MODULE ANALYZES PACKET FOR ERRORS
1612
OPERATING SYSTEM DEPENDENT MODULE REPLENISHES ADAPTER QUEUE WITH BUFFERS FROM FREE QUEUE
STOP
1600

FIG. 16

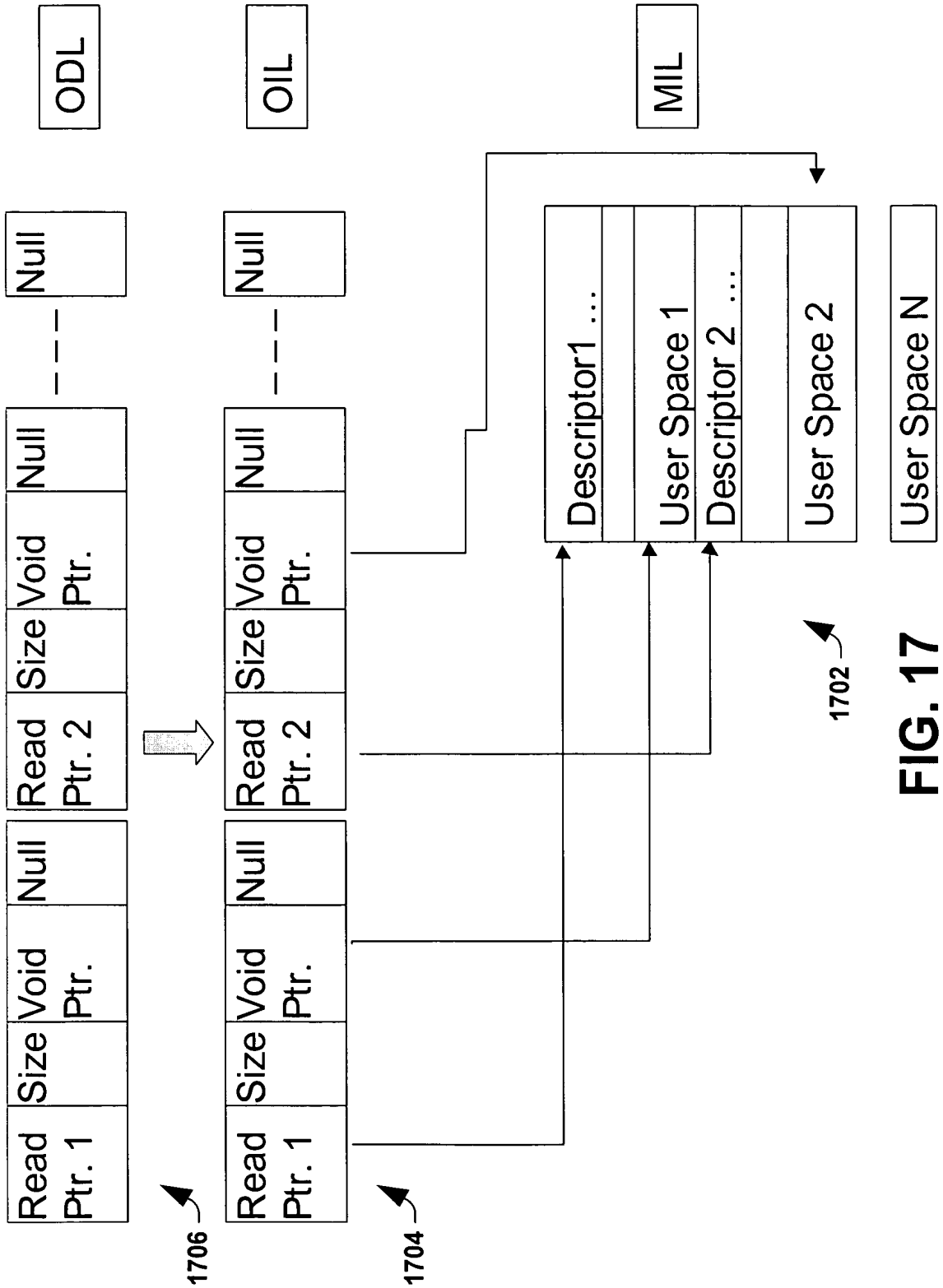
ODL
OIL
MIL
Null
Null
Read Ptr. 2
Size
Void Ptr.
Null
Read Ptr. 1
Size
Void Ptr.
Null
Descriptor1 ...
User Space 1
Descriptor 2 ...
User Space 2
User Space N
1706
1704
1702

FIG. 17

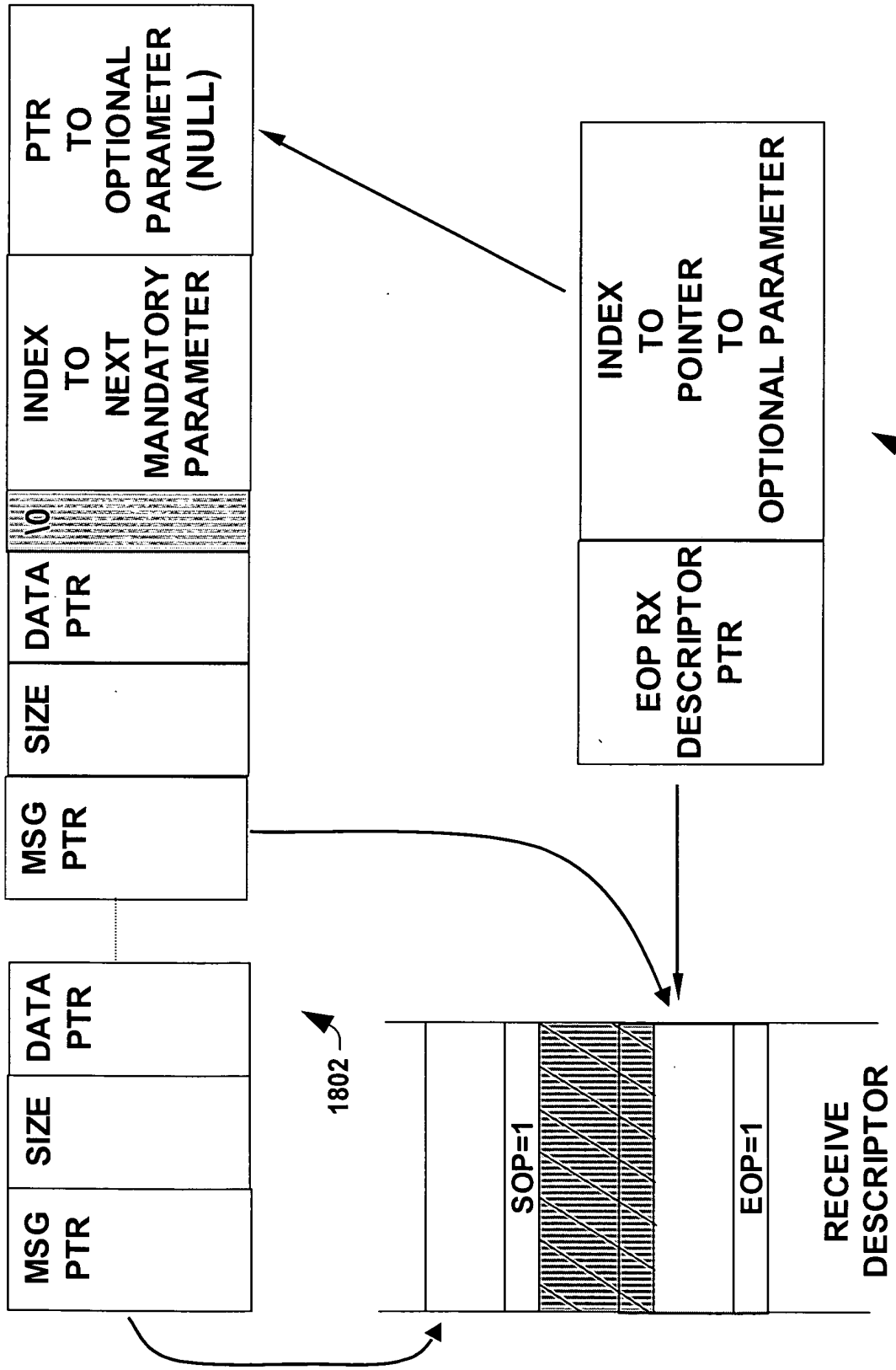
RECEIVE DESCRIPTOR
1801
SOP=1
EOP=1
1802
MSG PTR
SIZE
DATA PTR
MSG PTR
SIZE
DATA PTR
\0
INDEX TO NEXT MANDATORY PARAMETER
PTR TO OPTIONAL PARAMETER (NULL)
EOP RX DESCRIPTOR PTR
INDEX TO POINTER TO OPTIONAL PARAMETER
1804

FIG. 18

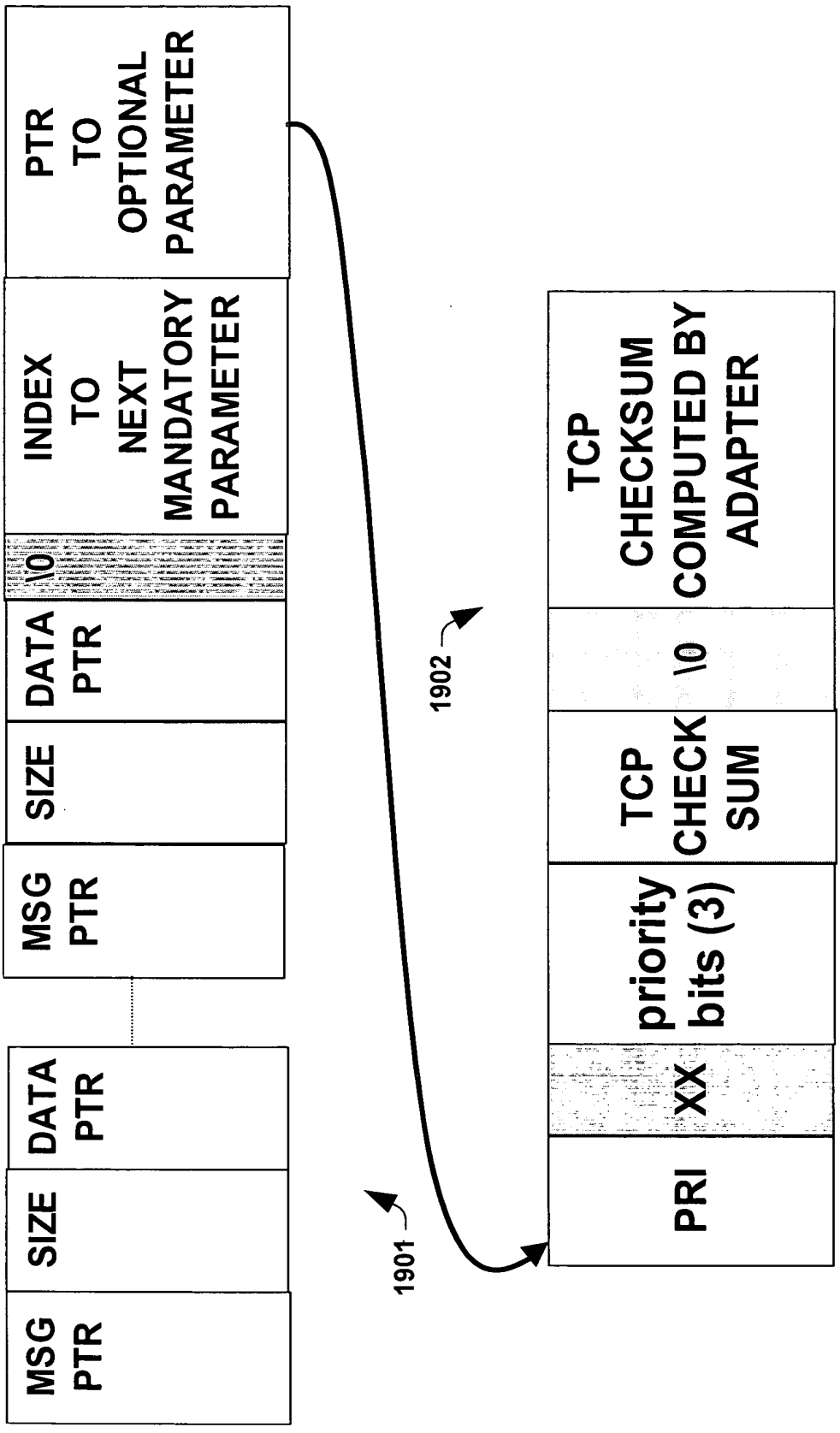
MSG PTR
SIZE
DATA PTR
MSG PTR
SIZE
DATA PTR
\0
INDEX TO NEXT MANDATORY PARAMETER
PTR TO OPTIONAL PARAMETER
1901
1902
PRI
XX
priority bits (3)
TCP CHECK SUM
\0
TCP CHECKSUM COMPUTED BY ADAPTER
1900

FIG. 19

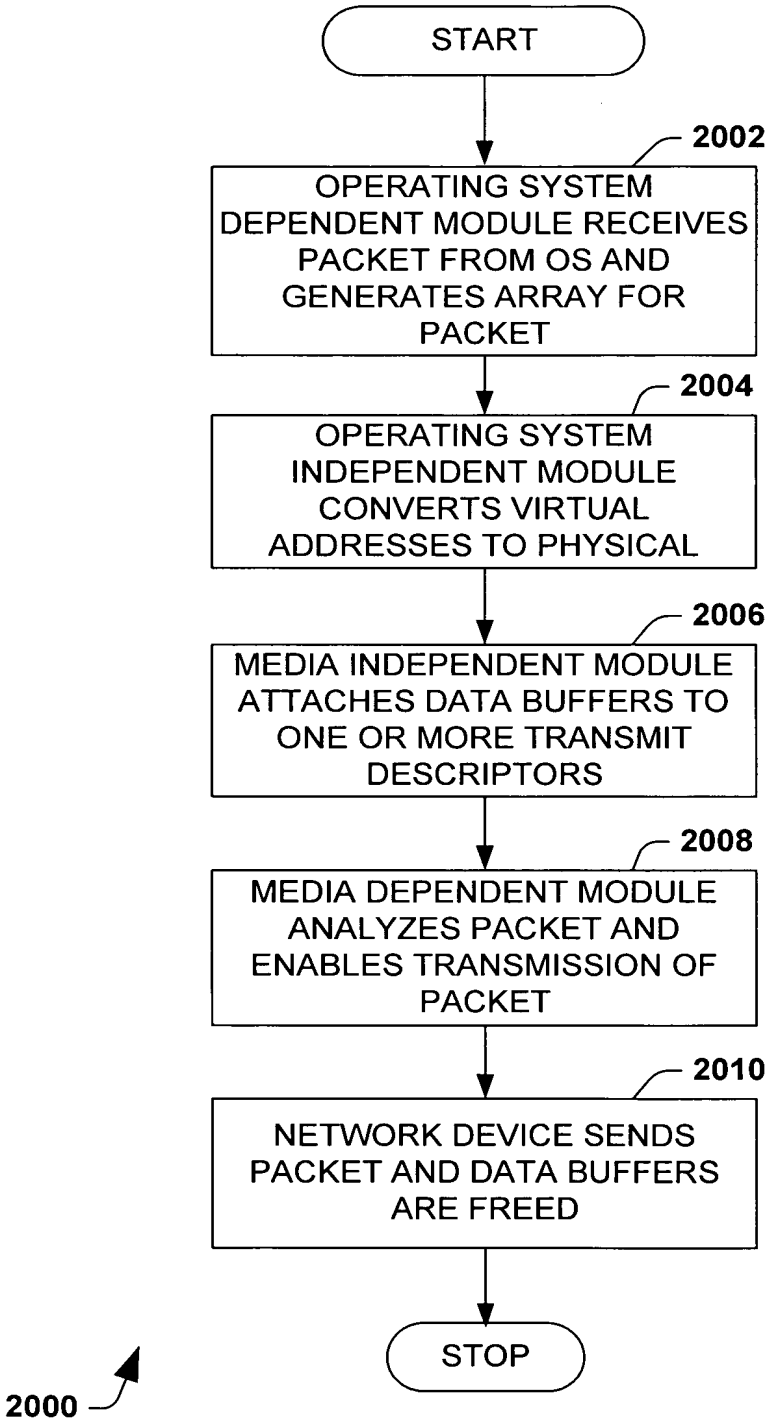
START
2002
OPERATING SYSTEM DEPENDENT MODULE RECEIVES PACKET FROM OS AND GENERATES ARRAY FOR PACKET
2004
OPERATING SYSTEM INDEPENDENT MODULE CONVERTS VIRTUAL ADDRESSES TO PHYSICAL
2006
MEDIA INDEPENDENT MODULE ATTACHES DATA BUFFERS TO ONE OR MORE TRANSMIT DESCRIPTORS
2008
MEDIA DEPENDENT MODULE ANALYZES PACKET AND ENABLES TRANSMISSION OF PACKET
2010
NETWORK DEVICE SENDS PACKET AND DATA BUFFERS ARE FREED
STOP
2000

FIG. 20

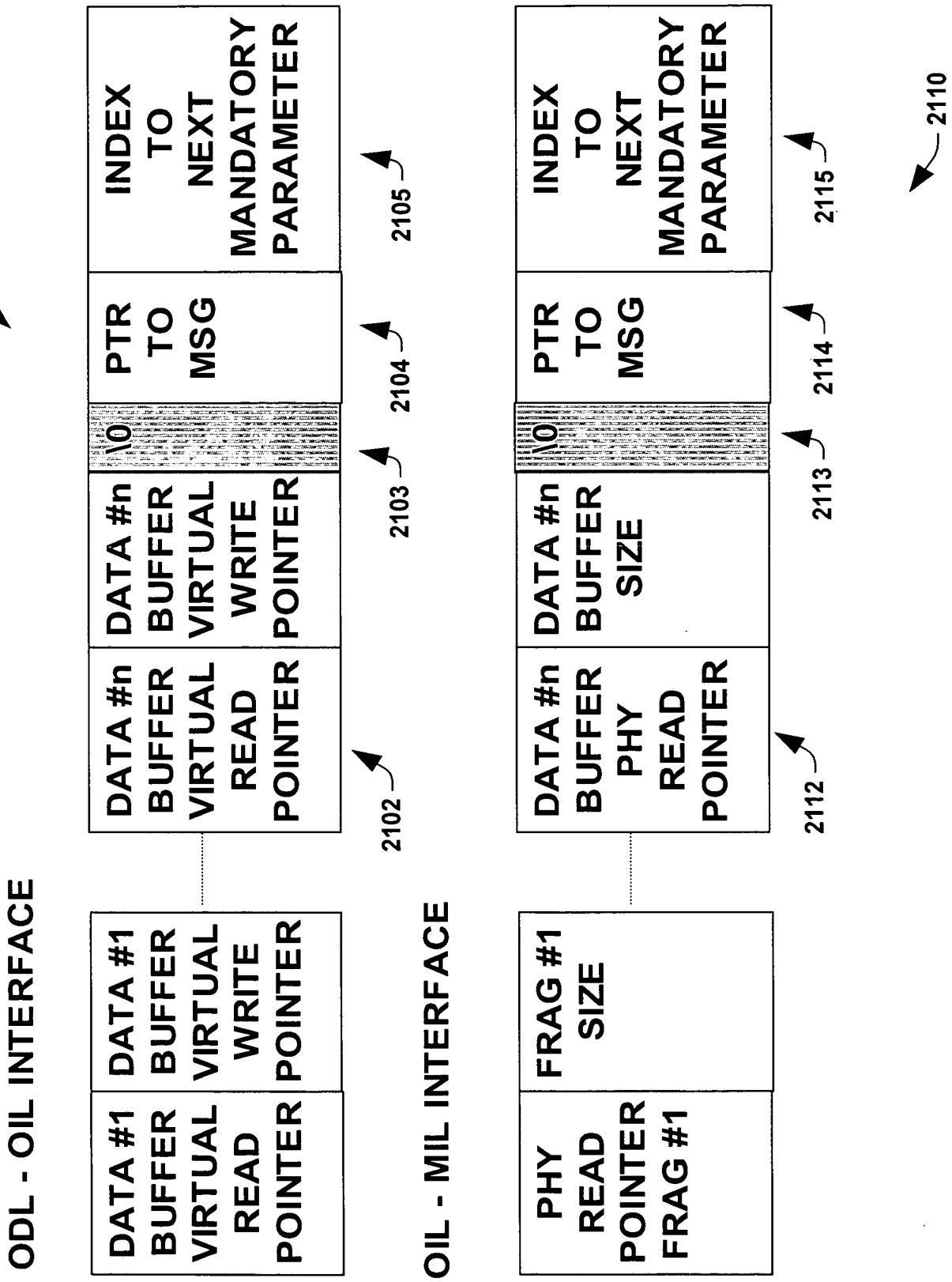
2101
ODL - OIL INTERFACE
DATA #1 BUFFER VIRTUAL READ POINTER
DATA #1 BUFFER VIRTUAL WRITE POINTER
DATA #n BUFFER VIRTUAL READ POINTER
DATA #n BUFFER VIRTUAL WRITE POINTER
\0
PTR TO MSG
INDEX TO NEXT MANDATORY PARAMETER
2102
2103
2104
2105
OIL - MIL INTERFACE
PHY READ POINTER FRAG #1
FRAG #1 SIZE
DATA #n BUFFER PHY READ POINTER
DATA #n BUFFER SIZE
\0
PTR TO MSG
INDEX TO NEXT MANDATORY PARAMETER
2112
2113
2114
2115
2110

FIG. 21

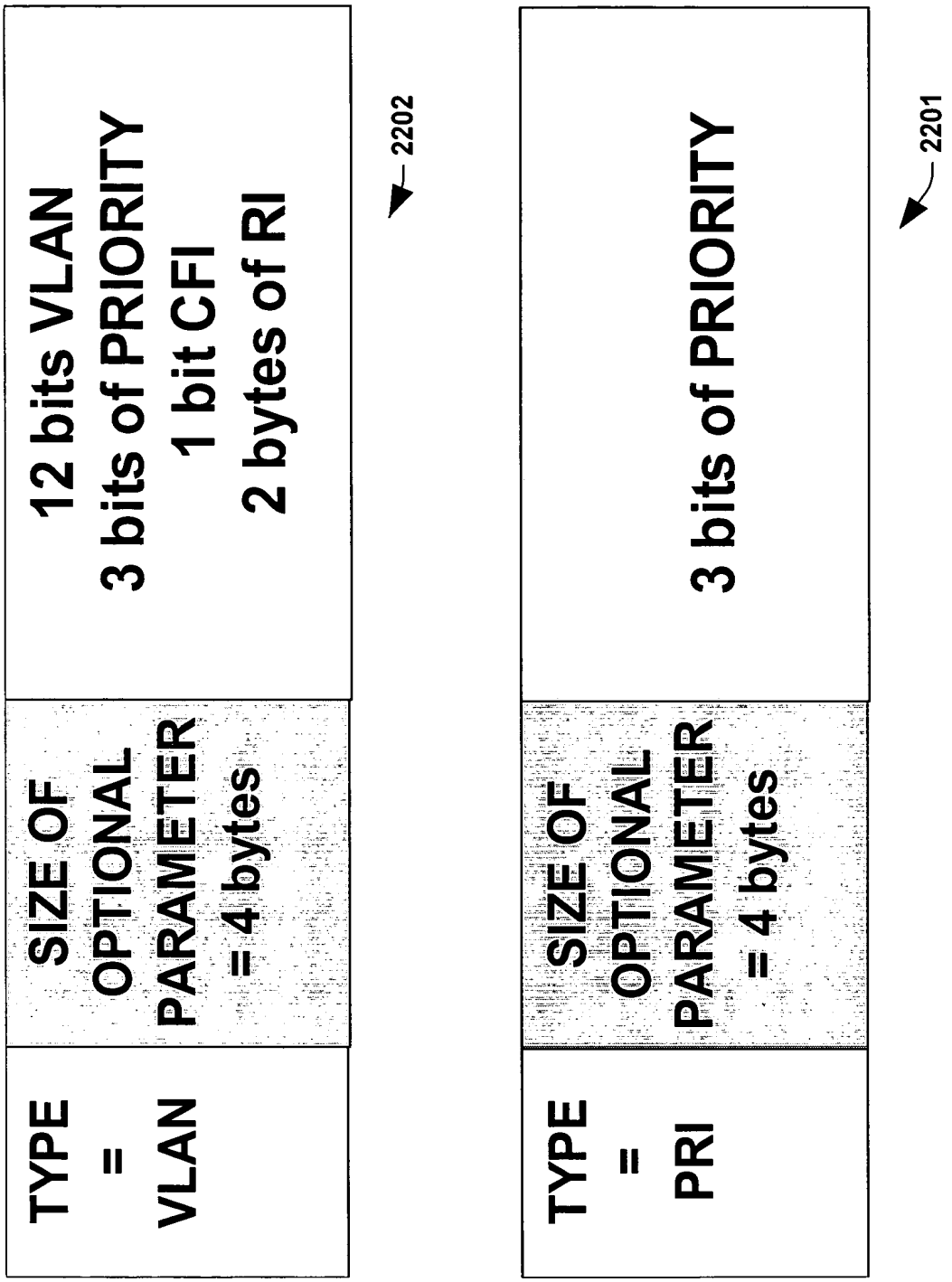
TYPE = VLAN
SIZE OF OPTIONAL PARAMETER = 4 bytes
12 bits VLAN
3 bits of PRIORITY
1 bit CFI
2 bytes of RI
2202
TYPE = PRI
SIZE OF OPTIONAL PARAMETER = 4 bytes
3 bits of PRIORITY
2201

FIG. 22

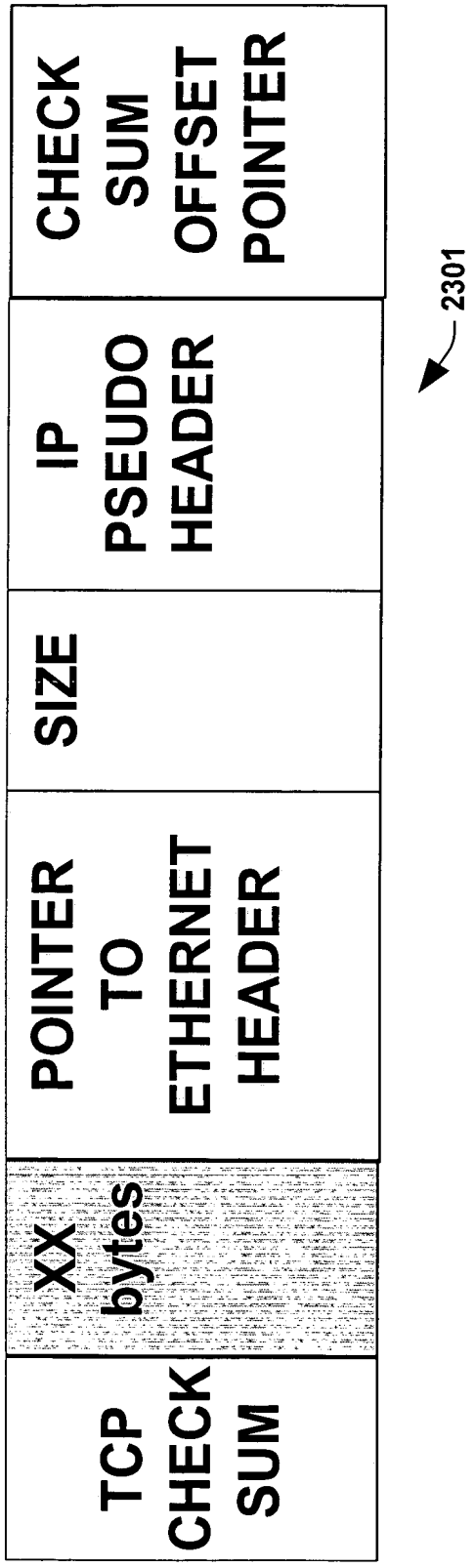
TCP CHECK SUM
XX bytes
POINTER TO ETHERNET HEADER
SIZE
IP PSEUDO HEADER
CHECK SUM OFFSET POINTER
2301
TCP CHECK SUM
XX bytes
TCP CHECKSUM COMPUTED BY ADAPTER
2302

FIG. 23

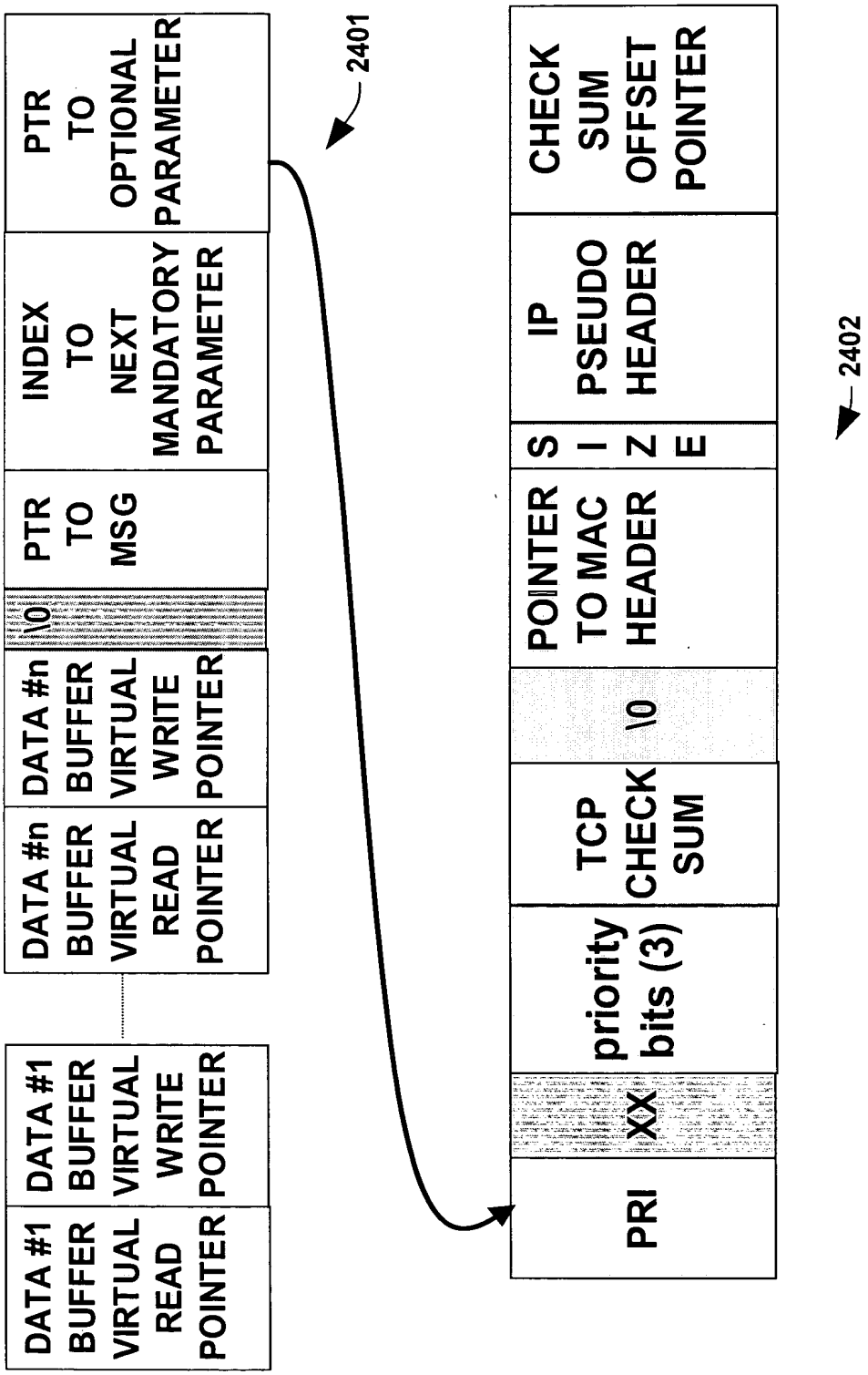
DATA #1 BUFFER VIRTUAL READ POINTER
DATA #1 BUFFER VIRTUAL WRITE POINTER
DATA #n BUFFER VIRTUAL READ POINTER
DATA #n BUFFER VIRTUAL WRITE POINTER
\0
PTR TO MSG
INDEX TO NEXT MANDATORY PARAMETER
PTR TO OPTIONAL PARAMETER
2401
PRI
XX
priority bits (3)
TCP CHECK SUM
\0
POINTER TO MAC HEADER
SIZE
IP PSEUDO HEADER
CHECK SUM OFFSET POINTER
2402

FIG. 24

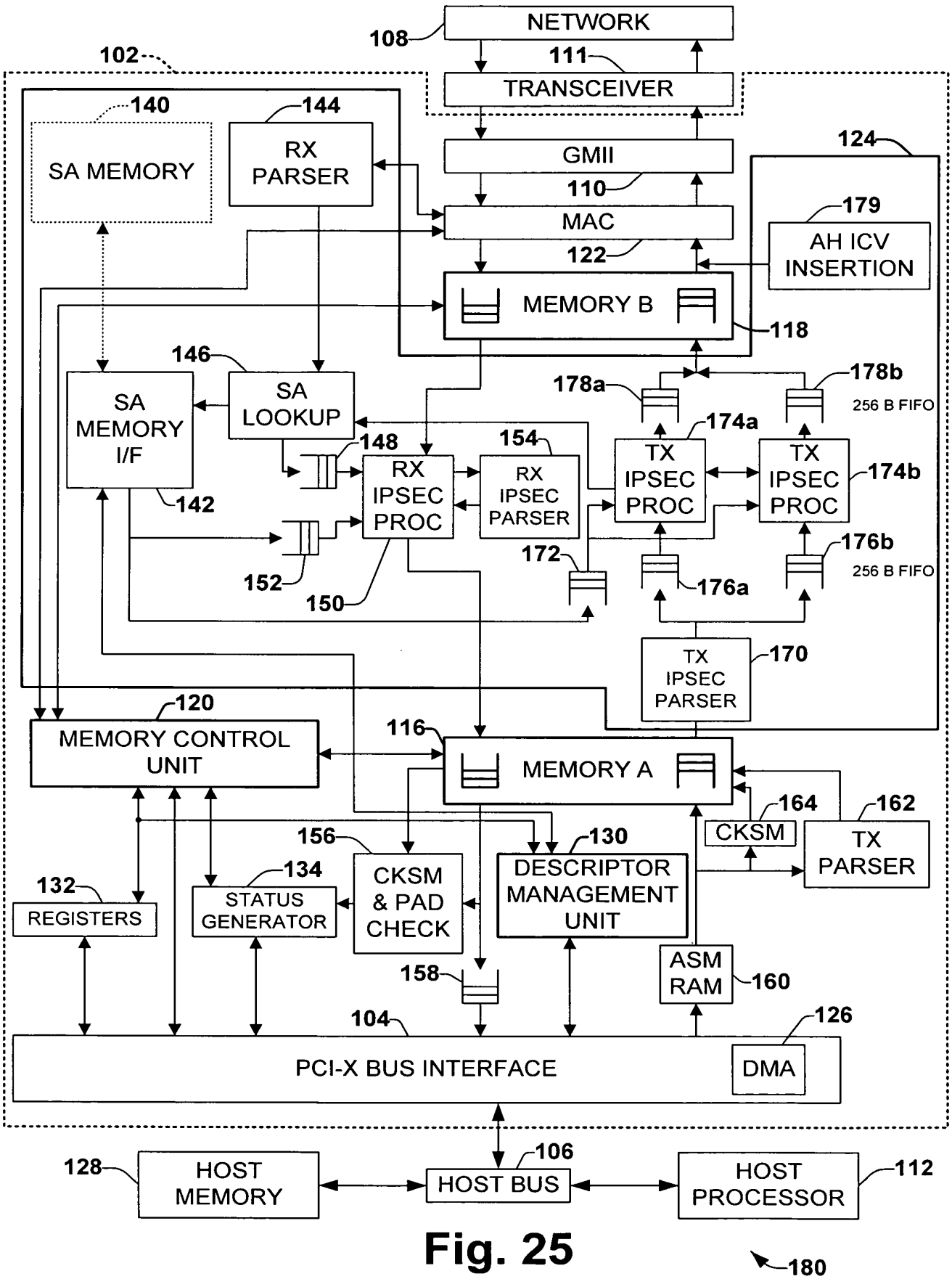
NETWORK
108
102
111
TRANSCEIVER
140
144
SA MEMORY
RX PARSER
GMII
124
110
MAC
179
AH ICV INSERTION
122
MEMORY B
118
146
SA LOOKUP
178a
178b
256 B FIFO
SA MEMORY I/F
148
154
174a
RX IPSEC PROC
RX IPSEC PARSER
TX IPSEC PROC
TX IPSEC PROC
174b
142
172
176b
256 B FIFO
152
150
176a
TX IPSEC PARSER
170
120
116
MEMORY CONTROL UNIT
MEMORY A
164
162
CKSM
TX PARSER
156
130
134
CKSM & PAD CHECK
DESCRIPTOR MANAGEMENT UNIT
132
REGISTERS
STATUS GENERATOR
158
ASM RAM
160
104
126
PCI-X BUS INTERFACE
DMA
106
128
HOST MEMORY
HOST BUS
HOST PROCESSOR
112
180

Fig. 25

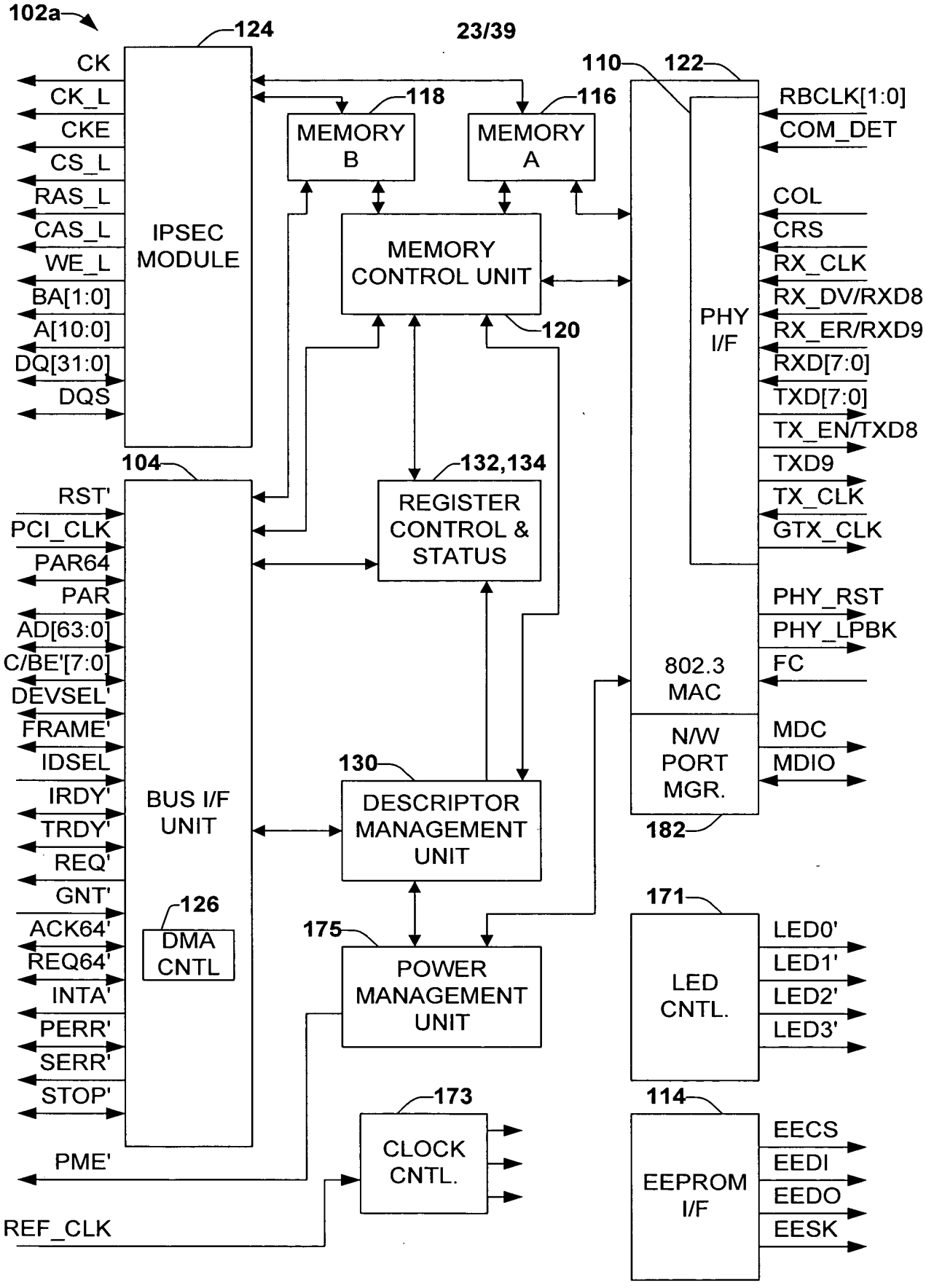
102a
124
IPSEC MODULE
CK
CK_L
CKE
CS_L
RAS_L
CAS_L
WE_L
BA[1:0]
A[10:0]
DQ[31:0]
DQS
118
MEMORY B
116
MEMORY A
MEMORY CONTROL UNIT
120
110
122
PHY I/F
RBCLK[1:0]
COM_DET
COL
CRS
RX_CLK
RX_DV/RXD8
RX_ER/RXD9
RXD[7:0]
TXD[7:0]
TX_EN/TXD8
TXD9
TX_CLK
GTX_CLK
104
132,134
REGISTER CONTROL & STATUS
RST'
PCI_CLK
PAR64
PAR
AD[63:0]
C/BE'[7:0]
DEVSEL'
FRAME'
IDSEL
IRDY'
TRDY'
REQ'
GNT'
ACK64'
REQ64'
INTA'
PERR'
SERR'
STOP'
BUS I/F UNIT
126
DMA CNTL
130
DESCRIPTOR MANAGEMENT UNIT
175
POWER MANAGEMENT UNIT
PHY_RST
PHY_LPBK
FC
802.3 MAC
N/W PORT MGR.
MDC
MDIO
182
171
LED CNTL.
LED0'
LED1'
LED2'
LED3'
173
CLOCK CNTL.
PME'
REF_CLK
114
EEPROM I/F
EECS
EEDI
EEDO
EESK

Fig. 26

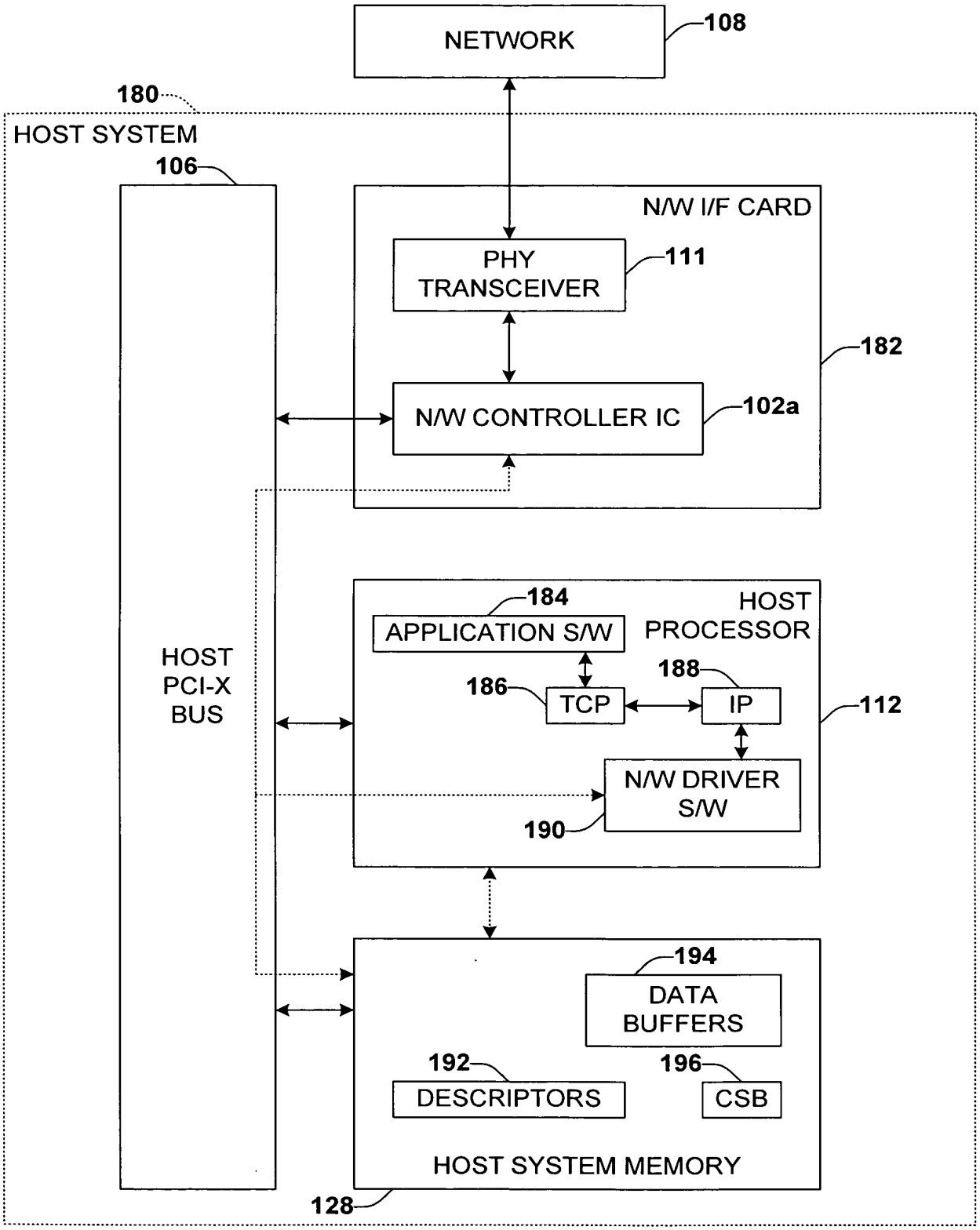
NETWORK
108
180
HOST SYSTEM
106
N/W I/F CARD
PHY
TRANSCEIVER
111
182
N/W CONTROLLER IC
102a
HOST
PCI-X
BUS
184
APPLICATION S/W
HOST
PROCESSOR
188
186
TCP
IP
112
N/W DRIVER
S/W
190
194
DATA
BUFFERS
192
196
DESCRIPTORS
CSB
HOST SYSTEM MEMORY
128

Fig. 27

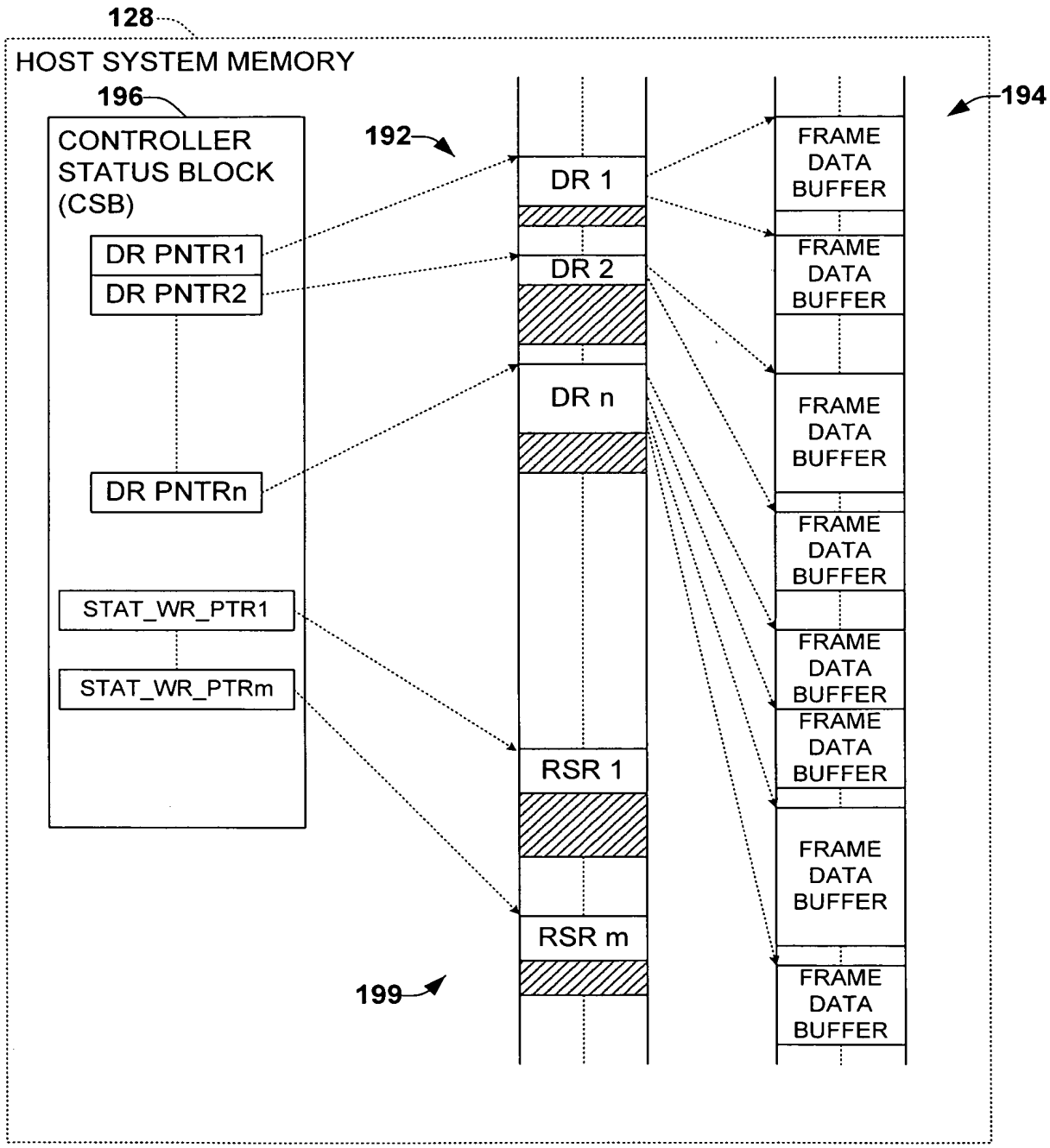
128
HOST SYSTEM MEMORY
196
CONTROLLER STATUS BLOCK (CSB)
DR PNTR1
DR PNTR2
DR PNTRn
STAT_WR_PTR1
STAT_WR_PTRm
192
DR 1
DR 2
DR n
RSR 1
RSR m
199
194
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER
FRAME DATA BUFFER

Fig. 28A

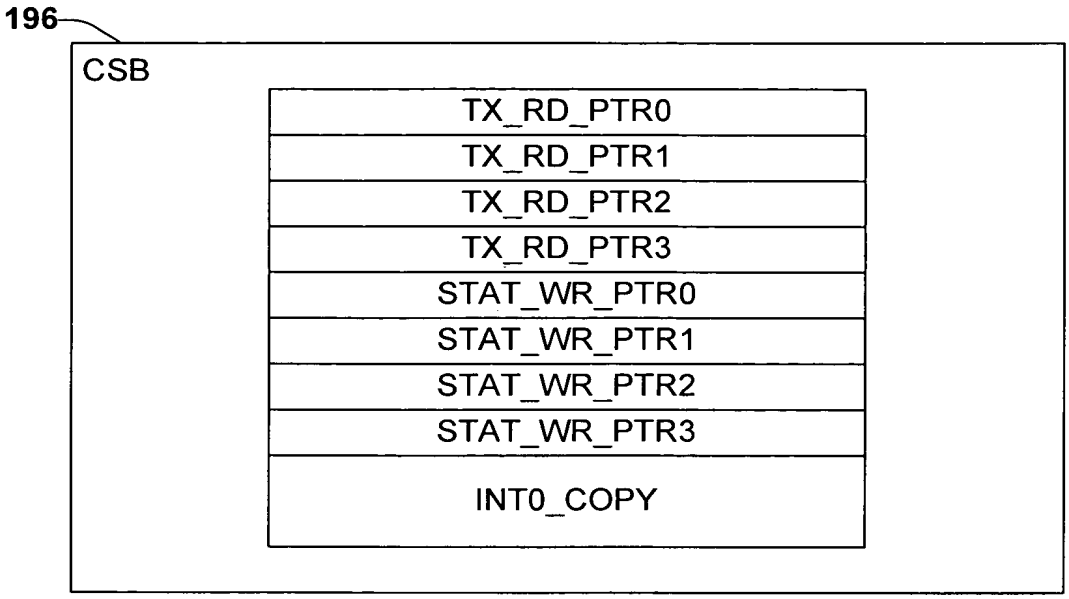

Fig. 28B

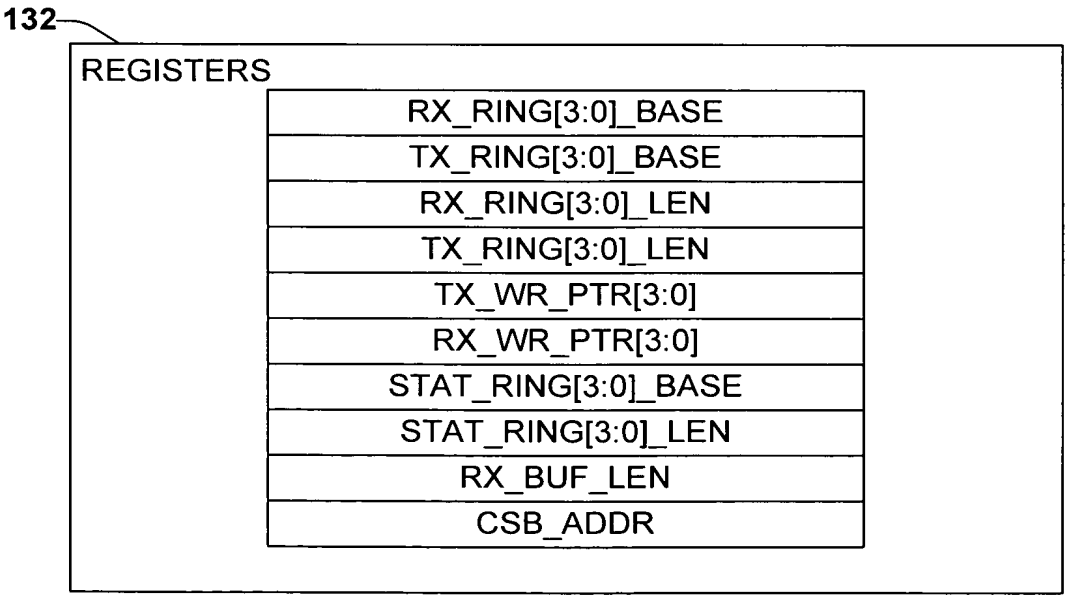

Fig. 28C

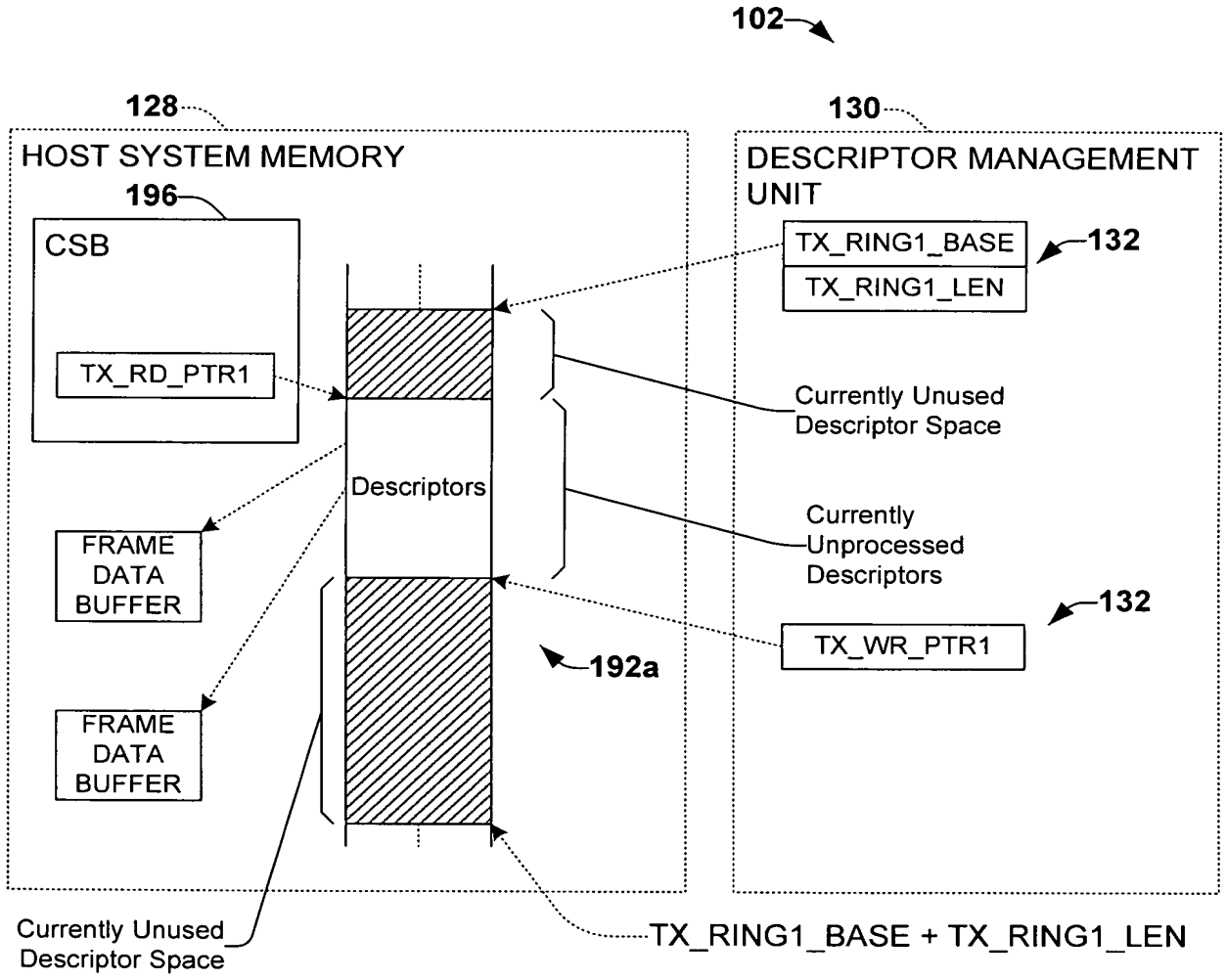
102
128
HOST SYSTEM MEMORY
196
CSB
TX_RD_PTR1
FRAME DATA BUFFER
FRAME DATA BUFFER
Descriptors
192a
Currently Unused Descriptor Space
130
DESCRIPTOR MANAGEMENT UNIT
TX_RING1_BASE
TX_RING1_LEN
132
Currently Unused Descriptor Space
Currently Unprocessed Descriptors
132
TX_WR_PTR1
TX_RING1_BASE + TX_RING1_LEN

Fig. 28D

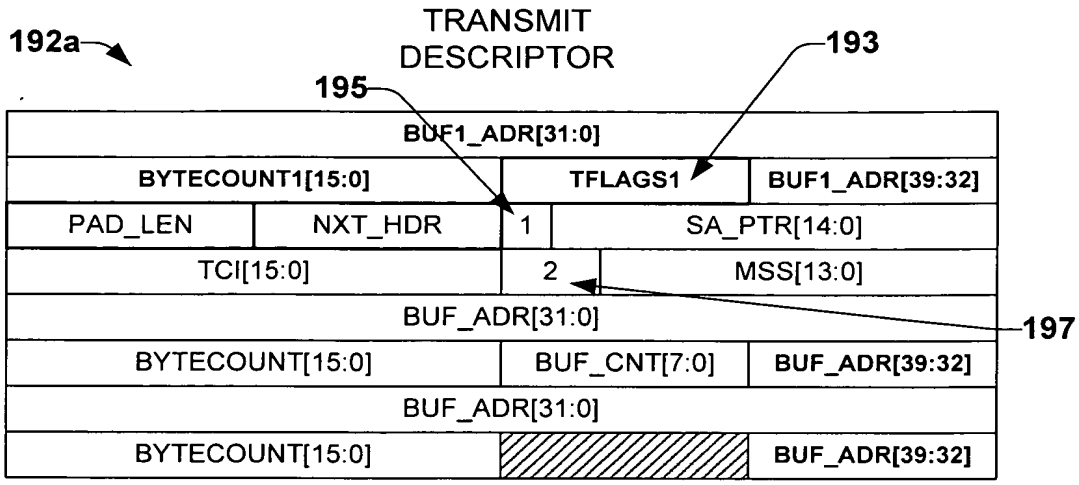

Fig. 28E

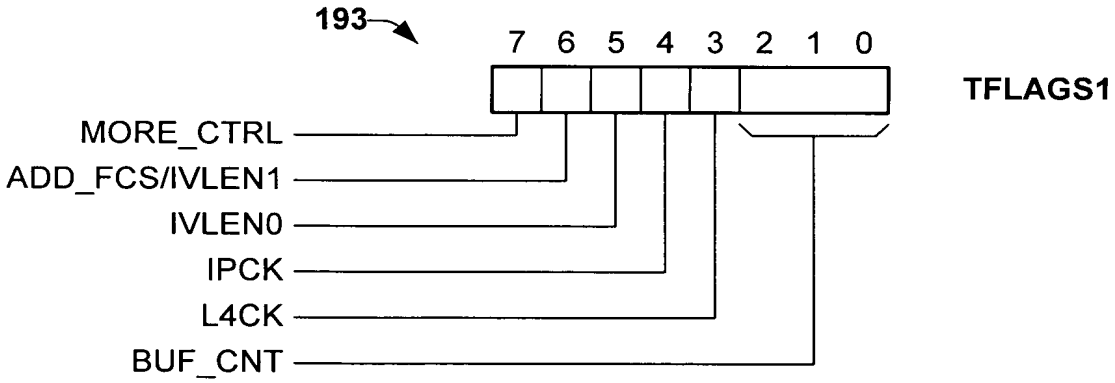

Fig. 28F

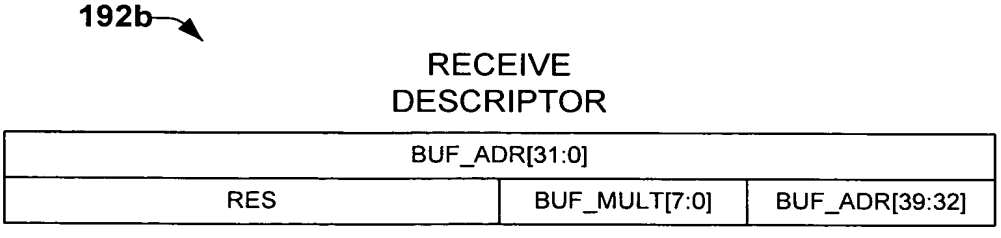

Fig. 28G

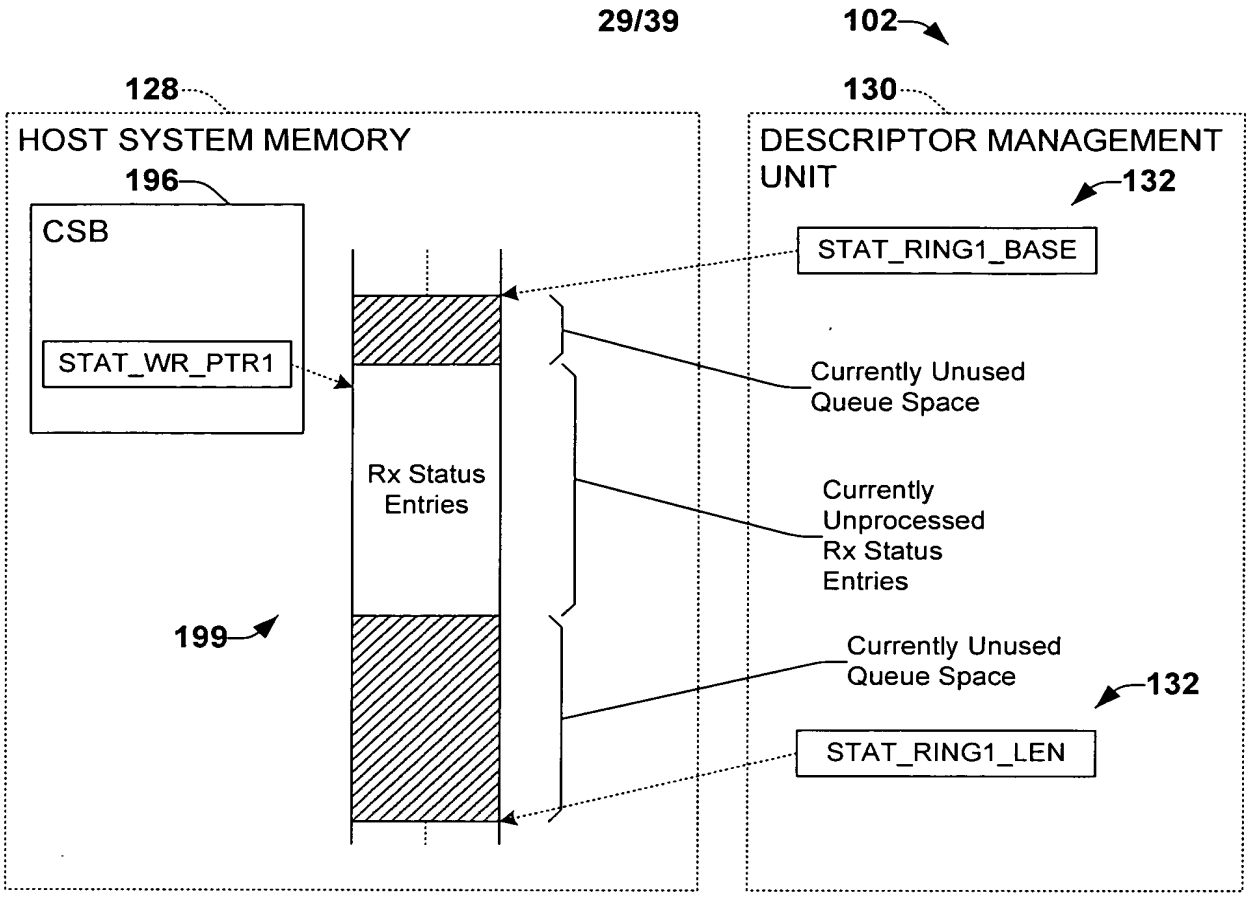

Fig. 28H

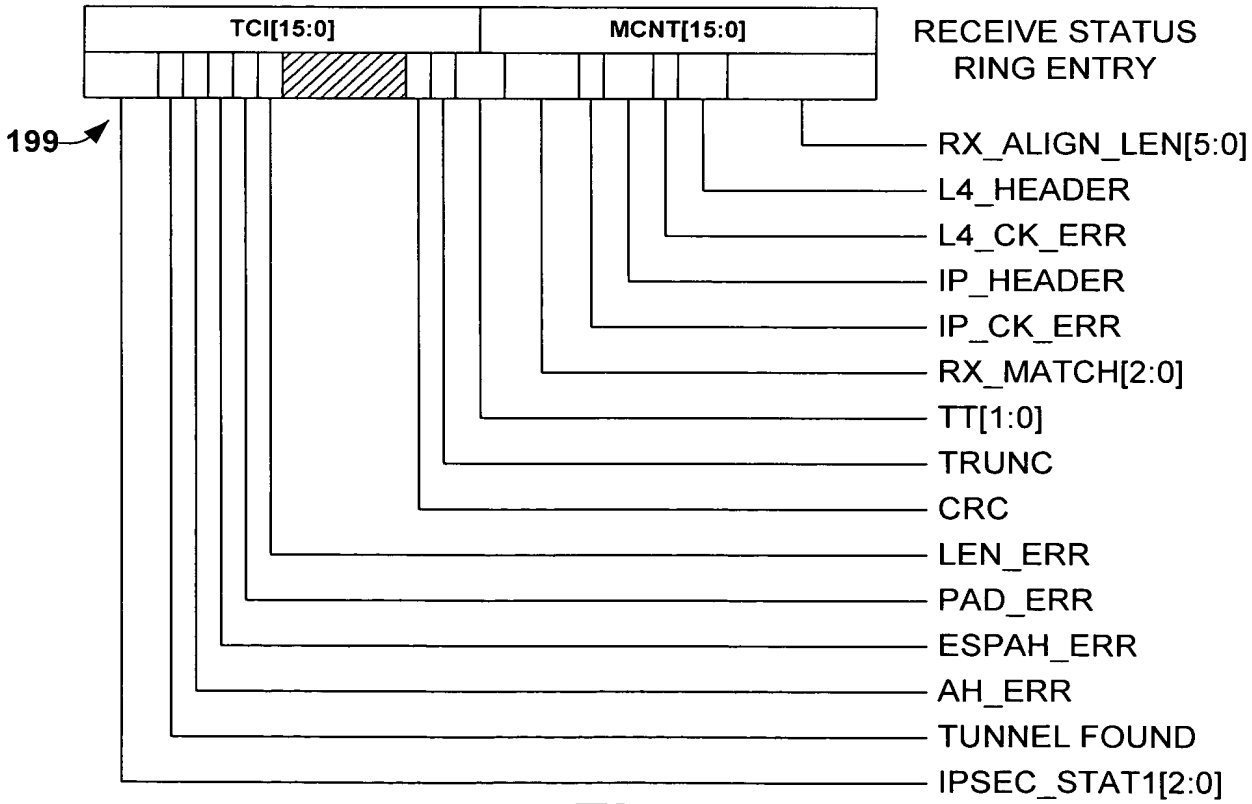

Fig. 28I

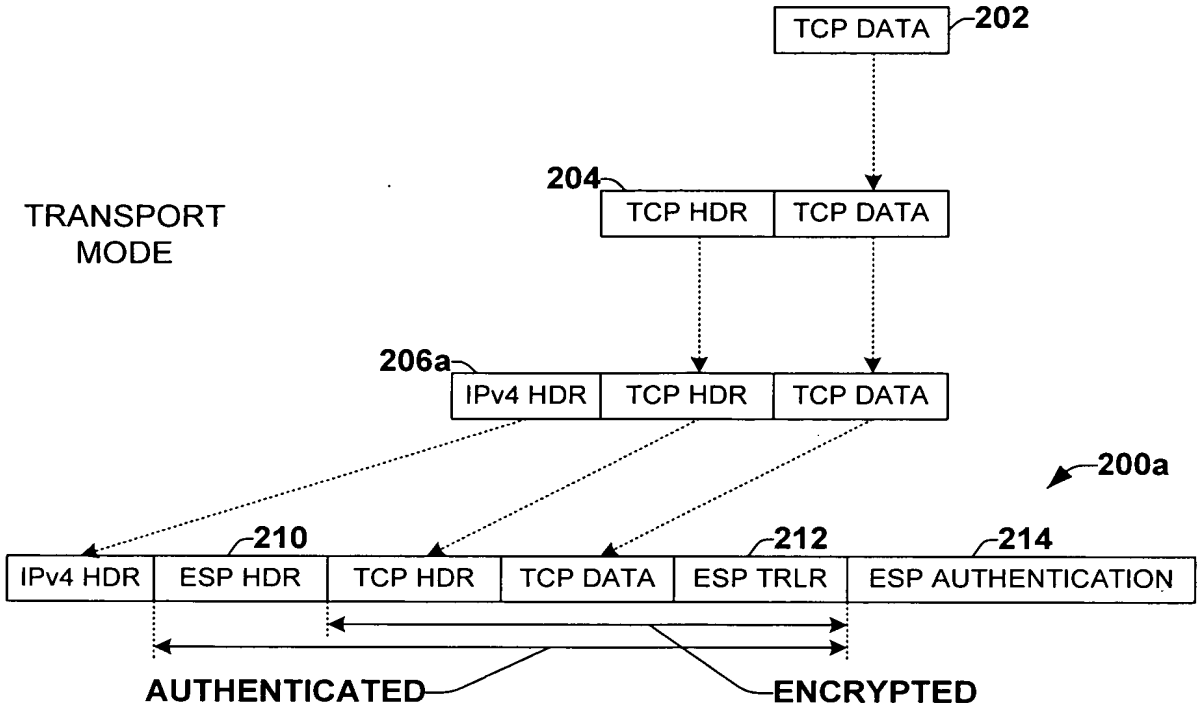

Fig. 29A

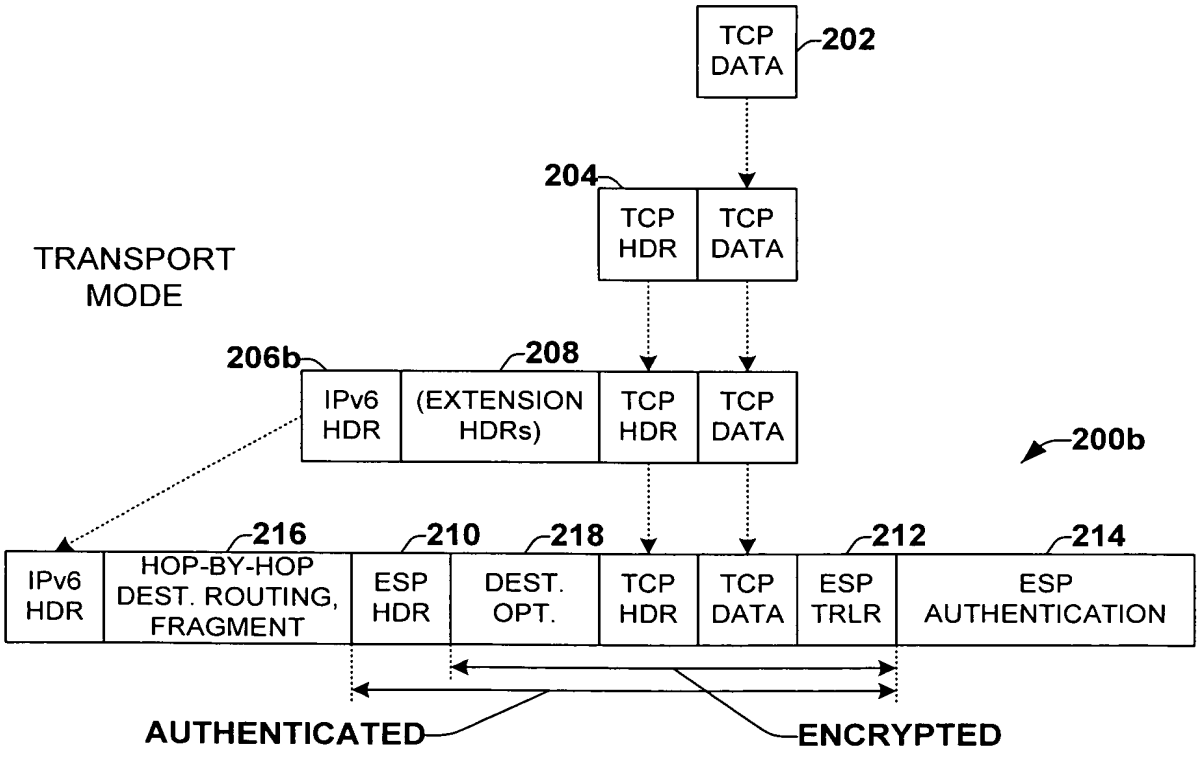

Fig. 29B

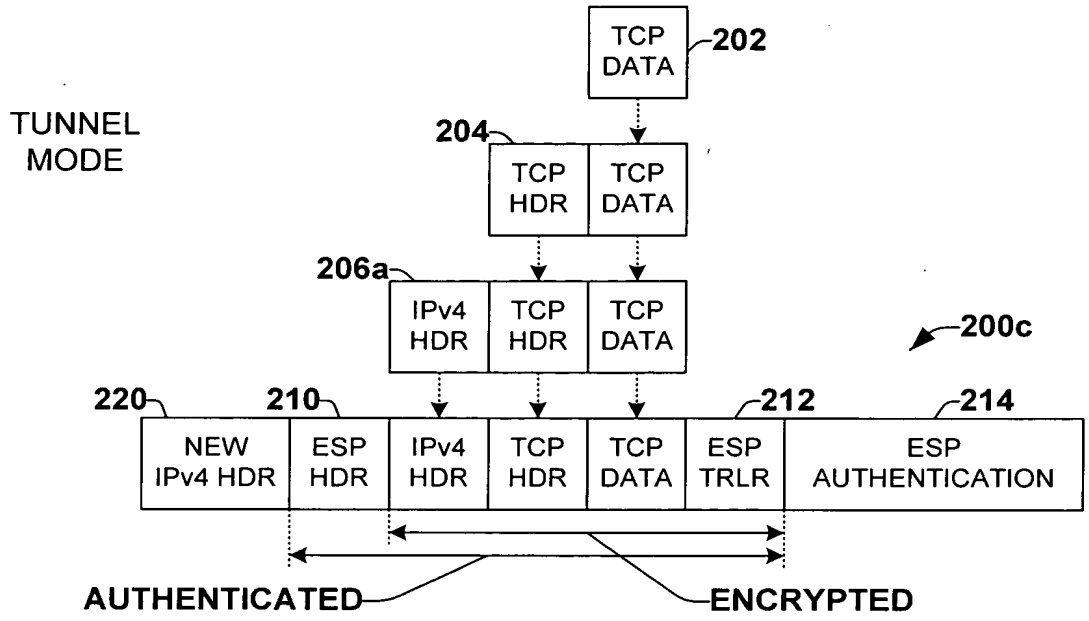

Fig. 29C

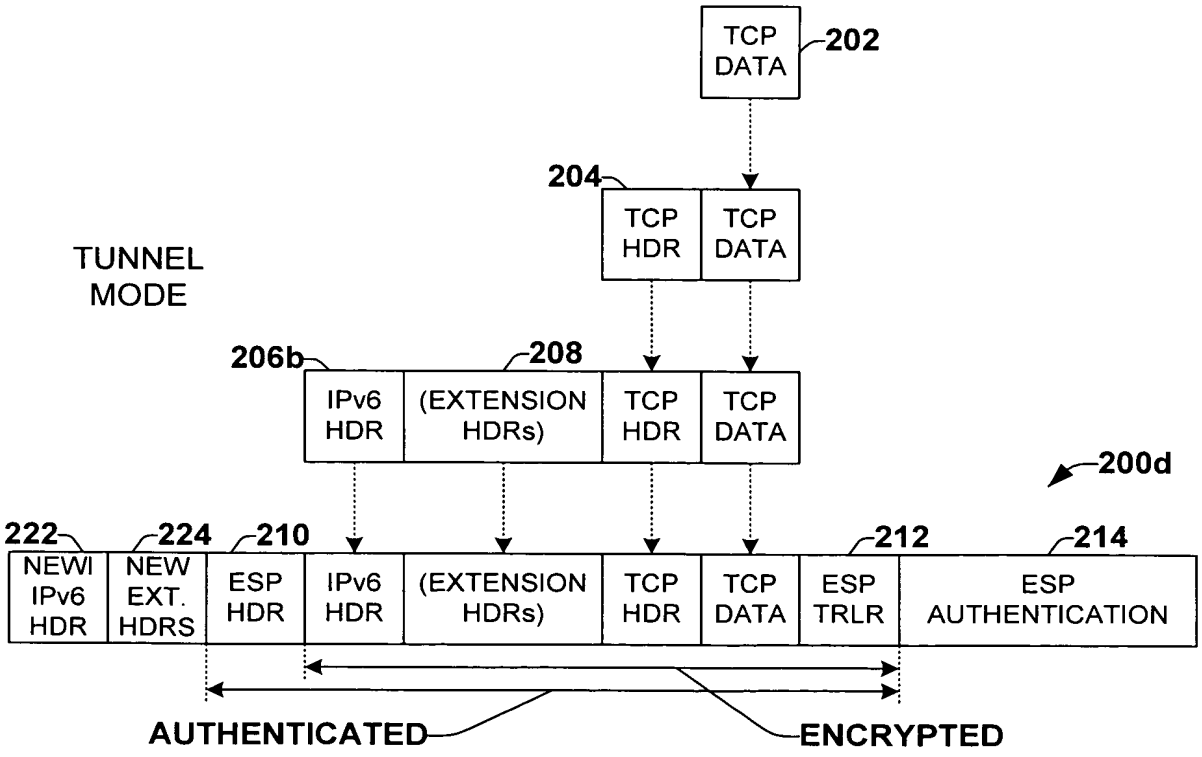

Fig. 29D

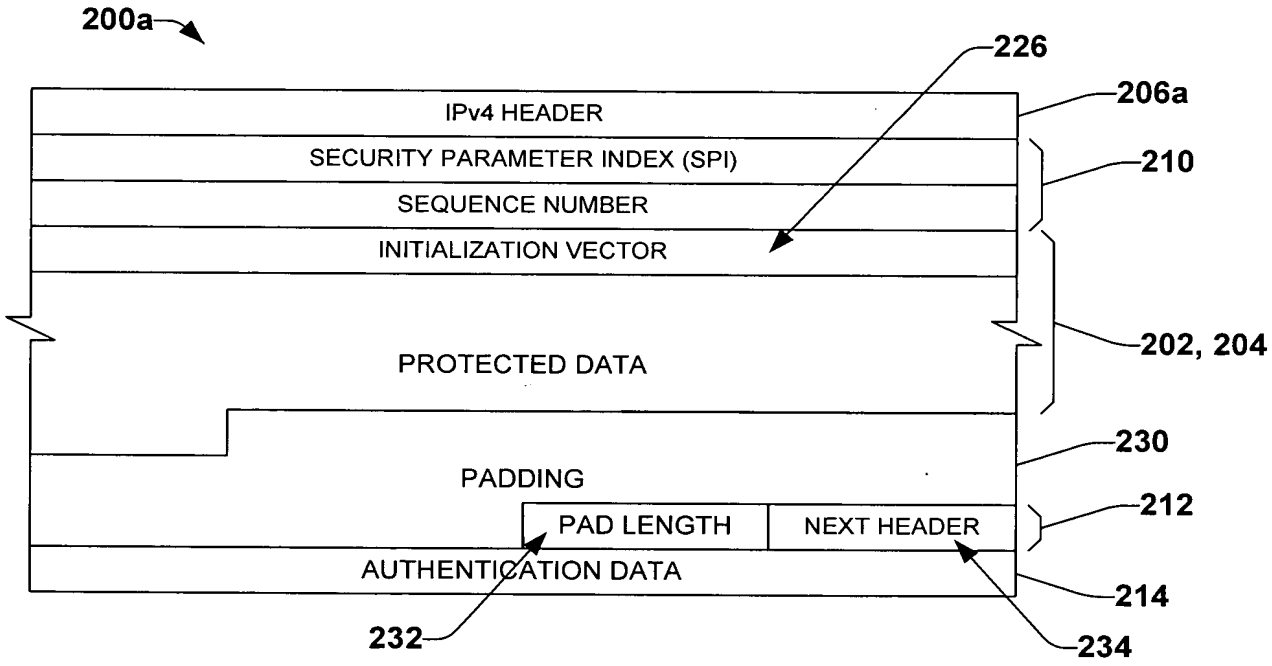
200a
226
206a
IPv4 HEADER
SECURITY PARAMETER INDEX (SPI)
210
SEQUENCE NUMBER
INITIALIZATION VECTOR
202, 204
PROTECTED DATA
230
PADDING
212
PAD LENGTH
NEXT HEADER
AUTHENTICATION DATA
214
232
234

Fig. 29E

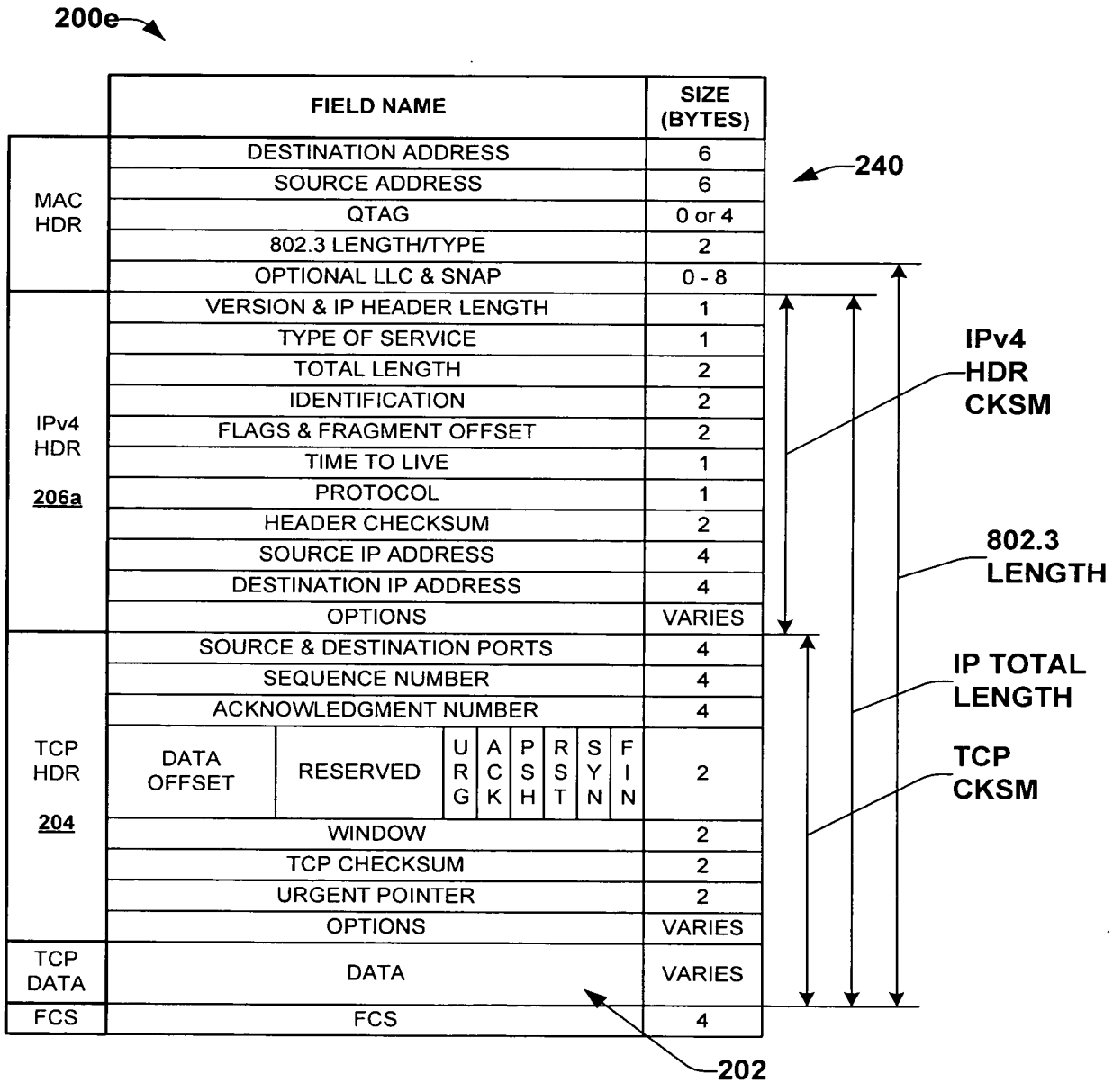
200e
FIELD NAME
SIZE (BYTES)
MAC HDR
DESTINATION ADDRESS 6
SOURCE ADDRESS 6
QTAG 0 or 4
802.3 LENGTH/TYPE 2
OPTIONAL LLC & SNAP 0 - 8
IPv4 HDR 206a
VERSION & IP HEADER LENGTH 1
TYPE OF SERVICE 1
TOTAL LENGTH 2
IDENTIFICATION 2
FLAGS & FRAGMENT OFFSET 2
TIME TO LIVE 1
PROTOCOL 1
HEADER CHECKSUM 2
SOURCE IP ADDRESS 4
DESTINATION IP ADDRESS 4
OPTIONS VARIES
TCP HDR 204
SOURCE & DESTINATION PORTS 4
SEQUENCE NUMBER 4
ACKNOWLEDGMENT NUMBER 4
DATA OFFSET
RESERVED
URG ACK PSH RST SYN FIN
2
WINDOW 2
TCP CHECKSUM 2
URGENT POINTER 2
OPTIONS VARIES
TCP DATA
DATA VARIES
FCS
FCS 4
240
IPv4 HDR CKSM
802.3 LENGTH
IP TOTAL LENGTH
TCP CKSM
202

Fig. 30A

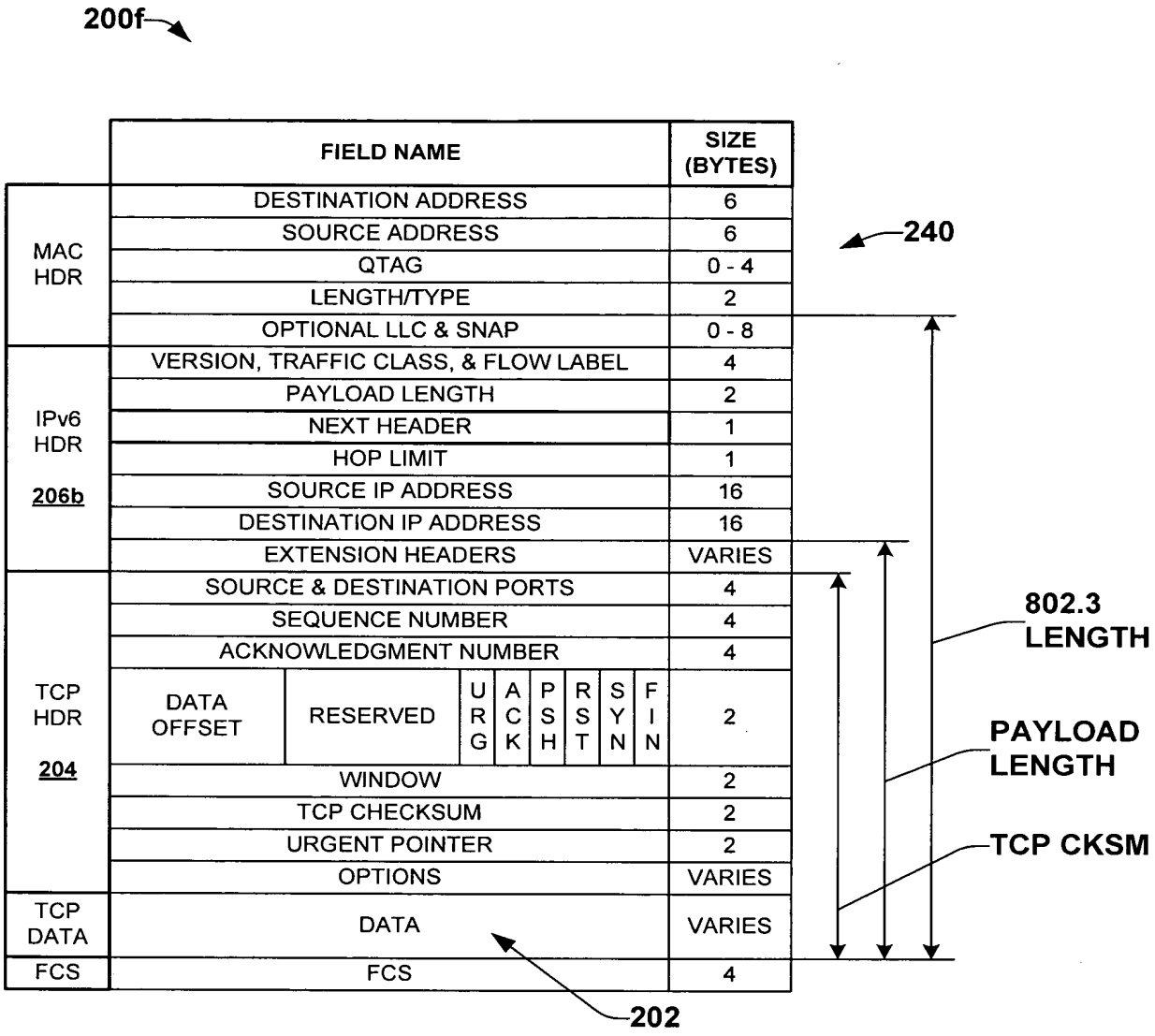
200f
FIELD NAME
SIZE (BYTES)
MAC HDR
DESTINATION ADDRESS 6
SOURCE ADDRESS 6
QTAG 0 - 4
LENGTH/TYPE 2
OPTIONAL LLC & SNAP 0 - 8
IPv6 HDR
206b
VERSION, TRAFFIC CLASS, & FLOW LABEL 4
PAYLOAD LENGTH 2
NEXT HEADER 1
HOP LIMIT 1
SOURCE IP ADDRESS 16
DESTINATION IP ADDRESS 16
EXTENSION HEADERS VARIES
TCP HDR
204
SOURCE & DESTINATION PORTS 4
SEQUENCE NUMBER 4
ACKNOWLEDGMENT NUMBER 4
DATA OFFSET
RESERVED
URG ACK PSH RST SYN FIN
2
WINDOW 2
TCP CHECKSUM 2
URGENT POINTER 2
OPTIONS VARIES
TCP DATA
DATA VARIES
FCS
FCS 4
240
802.3 LENGTH
PAYLOAD LENGTH
TCP CKSM
202

Fig. 30B

250

FIELD NAME	Created by Host	Modified by ESP	Encrypted	Covered by ESP Authentication	Added by Controller
Preamble					x
Start of Frame Delimiter					x
MAC Header	x				
IP Header	x				
ESP Header	x			x	
Payload Data	x	x	x	x	
Padding	x	x	x	x	
Pad Length	x	x	x	x	
Next Header	x	x	x	x	
Authentication Data	x	x			
Frame Check Sequence					x

Fig. 31A

252

FIELD NAME	Created by Host	Modified by AH Module	Covered by AH Authentication	Added by Controller
Preamble				x
Start of Frame Delimiter				x
MAC Header	x			
IP Header	x		x	
AH Header	x	x	x	
Other Headers	x		x	
Payload Data	x		x	
Frame Check Sequence				X

Fig. 31B

254

PHCKSM FOR IPv4	
32-BIT IP SOURCE ADDRESS	
32-BIT IP DESTINATION ADDRESS	
ZERO	PROTOCOL
TCP TOTAL LENGTH	

Fig. 31C

256

PHCKSM FOR IPv6	
128-BIT IP SOURCE ADDRESS	
128-BIT IP DESTINATION ADDRESS	
16-BIT TCP TOTAL LENGTH	
ZERO	PROTOCOL

Fig. 31D

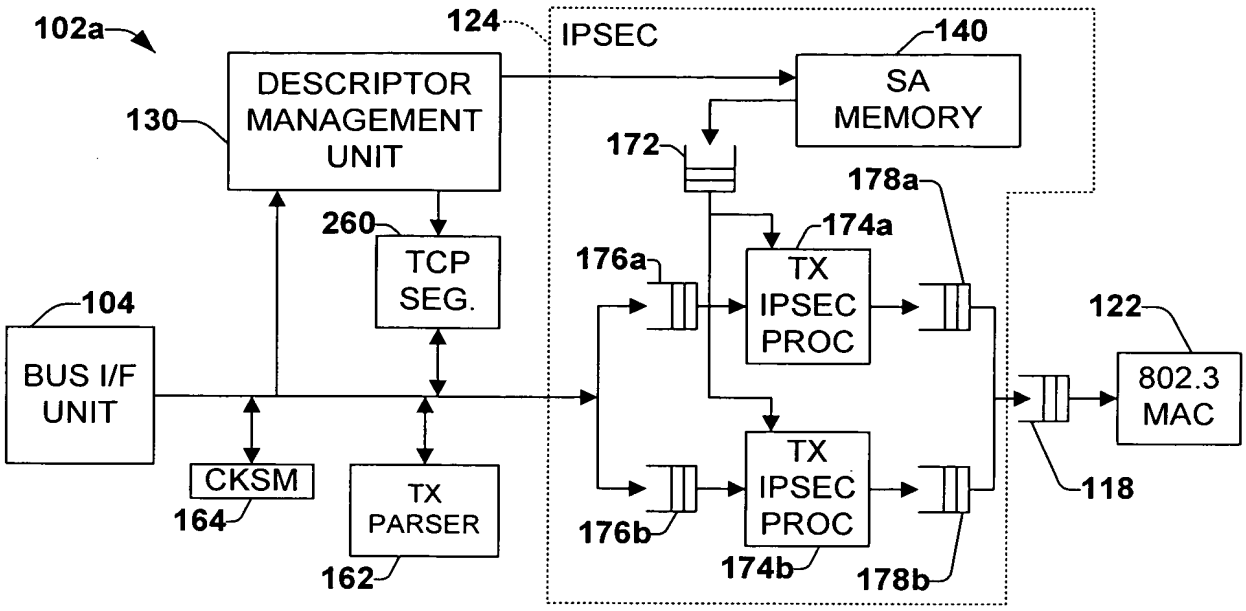
102a
124
IPSEC
140
SA MEMORY
DESCRIPTOR MANAGEMENT UNIT
130
172
178a
260
TCP SEG.
174a
176a
TX IPSEC PROC
104
122
BUS I/F UNIT
802.3 MAC
CKSM
164
TX PARSER
162
176b
TX IPSEC PROC
174b
178b
118

Fig. 32

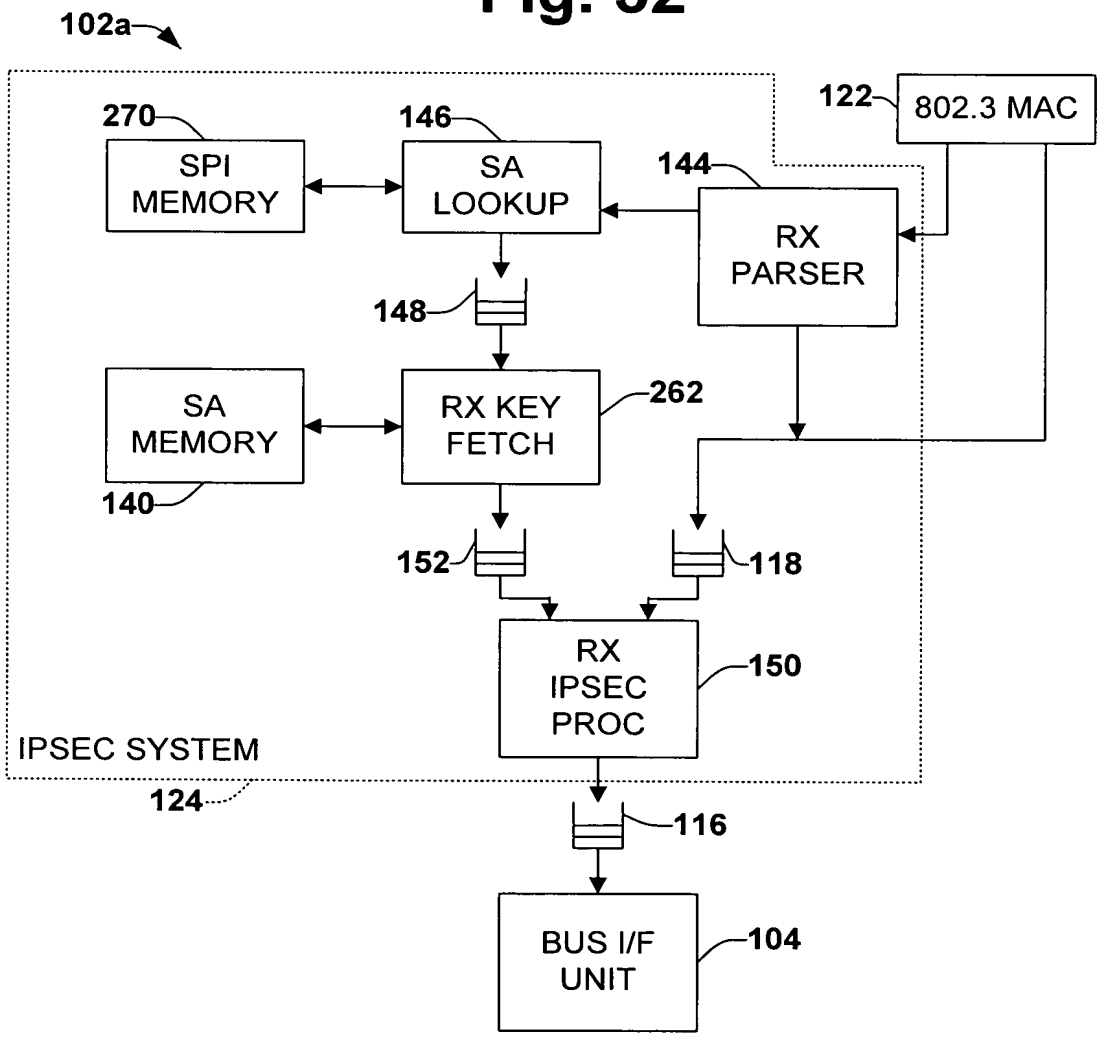
102a
122
802.3 MAC
270
SPI MEMORY
146
SA LOOKUP
144
RX PARSER
148
SA MEMORY
140
RX KEY FETCH
262
152
118
RX IPSEC PROC
150
IPSEC SYSTEM
124
116
BUS I/F UNIT
104

Fig. 33

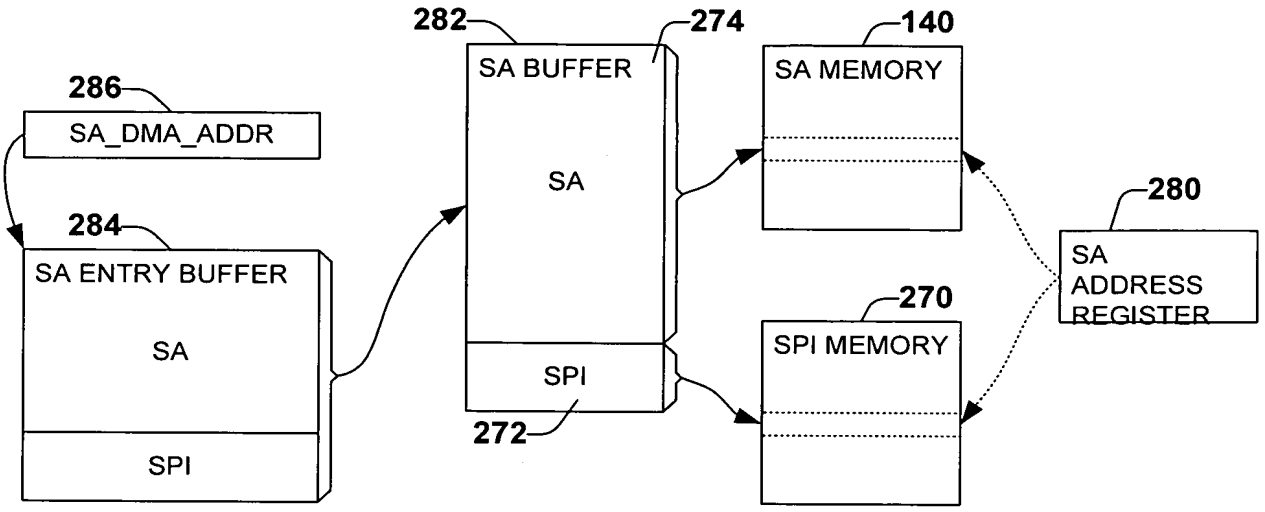

Fig. 34A

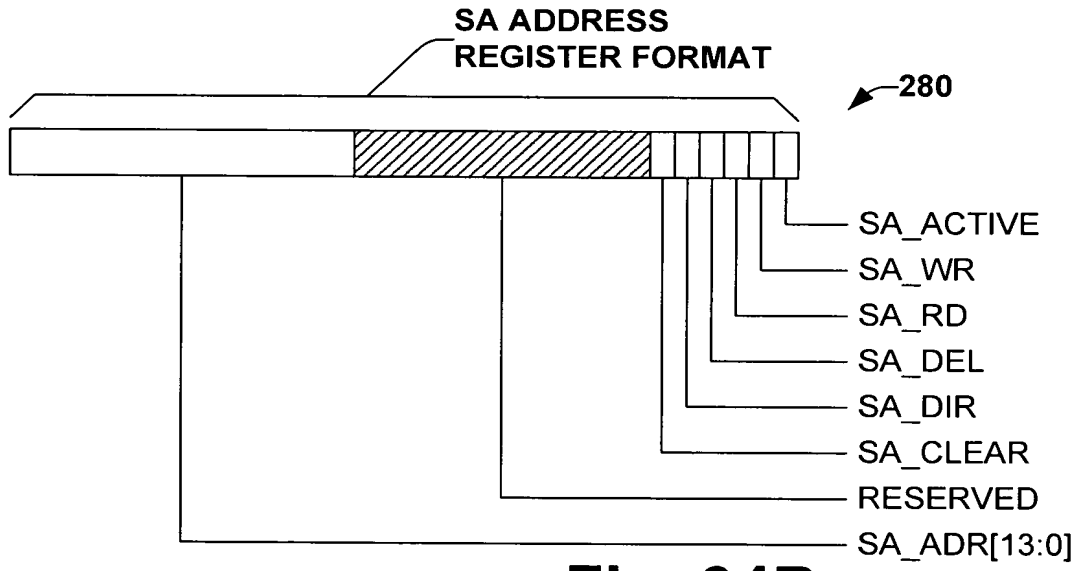

Fig. 34B

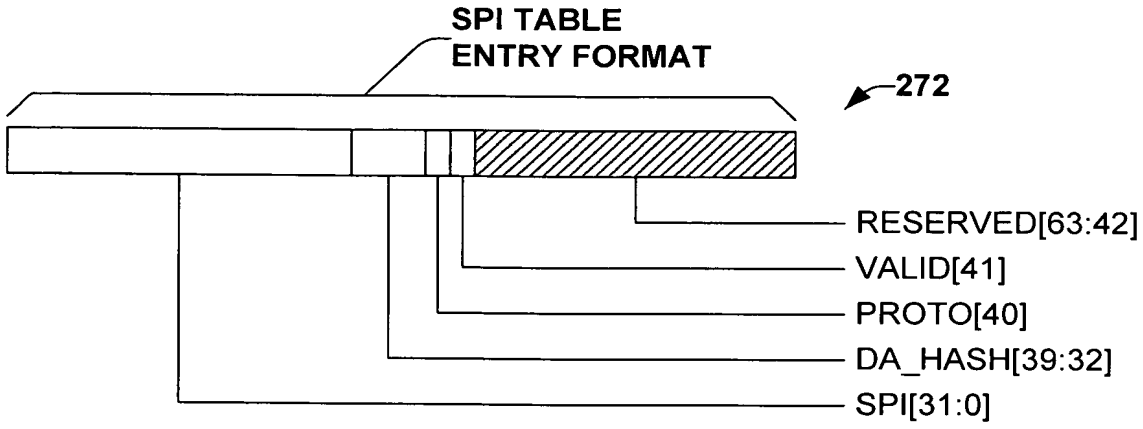

Fig. 34C

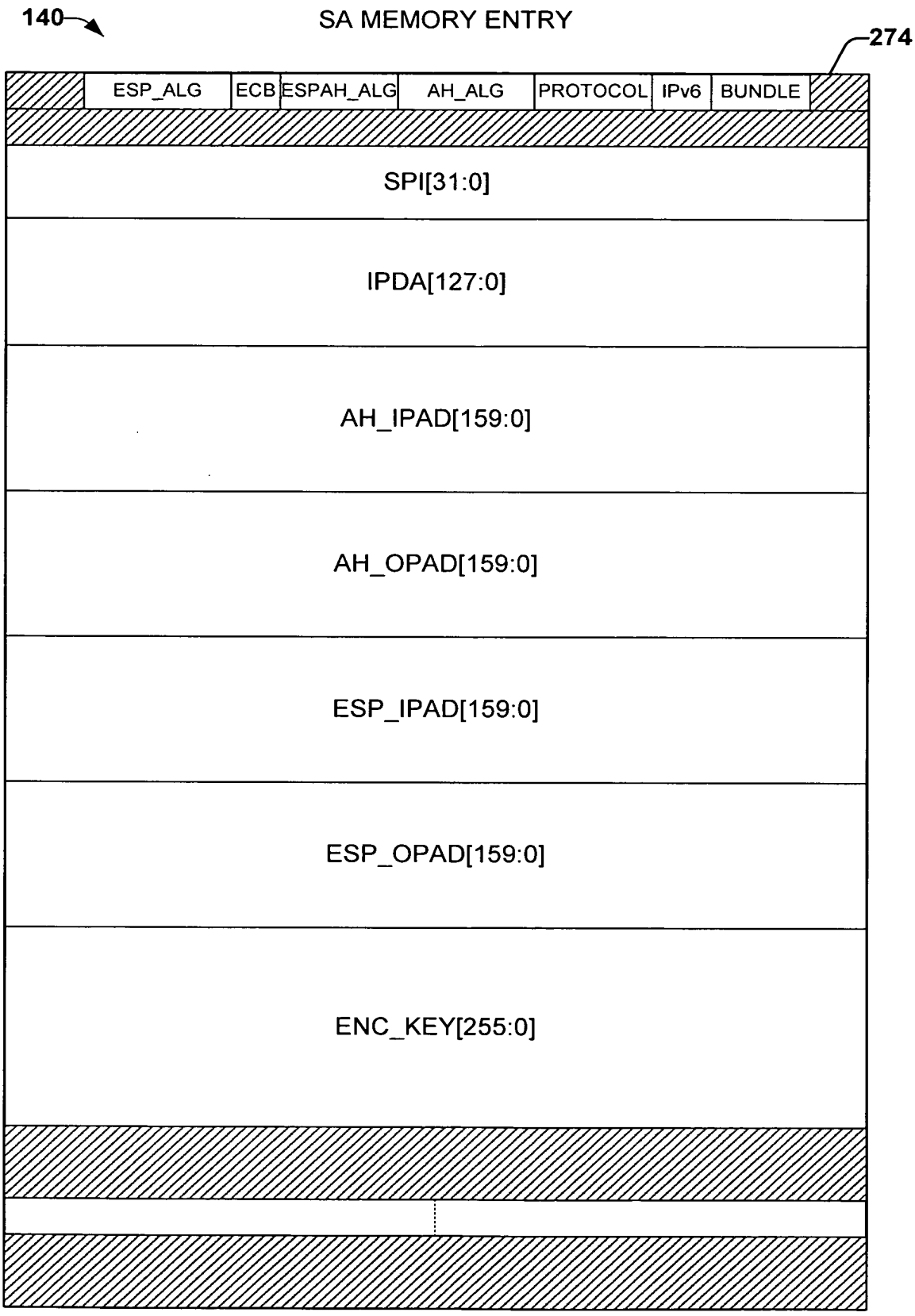
140
SA MEMORY ENTRY
274
ESP_ALG
ECB
ESPAH_ALG
AH_ALG
PROTOCOL
IPv6
BUNDLE
SPI[31:0]
IPDA[127:0]
AH_IPAD[159:0]
AH_OPAD[159:0]
ESP_IPAD[159:0]
ESP_OPAD[159:0]
ENC_KEY[255:0]

Fig. 34D